VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2018 – 19)

III SEMESTER

Sl. No	Course and Course Code		Course Title	Teaching Department	Teaching Hours /Week			Examination			
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks
					L	T	P				
1	BSC	18MAT31	Transform Calculus, Fourier Series and Numerical Techniques	Mathematics	2	2	--	03	40	60	100
2	PCC	18EC32	Network Theory		3	2	--	03	40	60	100
3	PCC	18EC33	Electronic Devices		3	0	--	03	40	60	100
4	PCC	18EC34	Digital System Design		3	0	--	03	40	60	100
5	PCC	18EC35	Computer Organization & Architecture		3	0	--	03	40	60	100
6	PCC	18EC36	Power Electronics & Instrumentation		3	0	--	03	40	60	100
7	PCC	18ECL37	Electronic Devices & Instrumentation Laboratory		--	2	2	03	40	60	100
8	PCC	18ECL38	Digital System DesignLaboratory		--	2	2	03	40	60	100
9	HSMC	18KVK39/49	Vyavaharika Kannada (Kannada for communication)/	HSMC	--	2	--	--	100	--	100
		18KAK39/49	Aadalitha Kannada (Kannada for Administration)								
		OR									
		18CPC39/49	Constitution of India, Professional Ethics and Cyber Law		1	--	--	03	40	60	
					Examination is by objective type questions						
				TOTAL	17 OR 18	10 OR 08	04	24 OR 27	420 OR 360	480 OR 540	900

Note: BSC: Basic Science, PCC: Professional Core, HSMC: Humanity and Social Science, NCMC: Non-credit mandatory course.

18KVK39Vyavaharika Kannada (Kannada for communication) is for non-kannada speaking, reading and writing students and 18KAK39 Aadalitha Kannada (Kannada for Administration) is for students who speak, read and write kannada.

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

10	NCMC	18MATDIP31	Additional Mathematics - I	Mathematics	02	01	--	03	40	60	100

(a)The mandatory non – credit courses Additional Mathematics I and II prescribed for III and IV semesters respectively, to the lateral entry Di holders admitted to III semester of BE/B.Tech programs,shall attend the classes during therespective semesters to complete all the formalities course and appear for the University examination.In case, any student fails to register for the said course/fails to secure the minimum 40 % prescribed CIE marks, he/she shall be deemed to have secured F grade. In such a case, the students have to fulfill the requirements during subs semester/s to appear for SEE.

(b)These Courses shall not beconsidered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

Courses prescribed to lateral entry B. Sc degree holders admitted to III semester of Engineering programs

Lateral entrant students from B.Sc. Stream, shall clear the non-credit courses Engineering Graphics and Elements of Civil Engineerin Mechanics of the First Year Engineering Programme. These Courses shall not be considered for vertical progression, but completion of the c shall be mandatory for the award of degree.

AICTE Activity Points to be earned by students admitted to BE/B.Tech/B.Plan day college programme (For more details refer to Ch 6,AICTE Activity Point Programme, Model Internship Guidelines):

Over and above the academic grades, every Day College regular student admitted to the 4 years Degree programme and every student entering 4 Degree programme through lateral entry, shall earn 100 and 75 Activity Points respectively for the award of degree through AICTE Activity Programme. Students transferred from other Universities to fifth semester are required to earn 50 Activity Points from the year of entry to VTU Activity Points earned shall be reflected on the student's eighth semester Grade Card.

The activities can be can be spread over the years, anytime during the semester weekends and holidays, as per the liking and convenience of the s from the year of entry to the programme. However, minimum hours' requirement should be fulfilled. Activity Points (non-credit) have no effe SGPA/CGPA and shall not be considered for vertical progression.

In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity P Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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EMESTER

	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
	BSC	18MAT41	Complex Analysis, Probability and Statistical Methods	Mathematics	2	2	--	03	40	60	100	3
	PCC	18EC42	Analog Circuits		3	2	--	03	40	60	100	4
	PCC	18EC43	Control Systems		3	0	--	03	40	60	100	3
	PCC	18EC44	Engineering Statistics & Linear Algebra		3	0	--	03	40	60	100	3
	PCC	18EC45	Signals & Systems		3	0	--	03	40	60	100	3
	PCC	18EC46	Microcontroller		3	0	--	03	40	60	100	3
	PCC	18ECL47	Microcontroller Laboratory		--	2	2	03	40	60	100	2
	PCC	18ECL48	Analog Circuits Laboratory		--	2	2	03	40	60	100	2
	HSMC	18KVK39/49	Vyavaharika Kannada (Kannada for communication)	HSMC	--	2	--	--	100	--	100	1
		18KAK39/49	Aadalitha Kannada (Kannada for Administration)									
			OR									
		18CPC39/49	Constitution of India, Professional Ethics and Cyber Law		1	--	--	03	40	60		
					Examination is by objective type questions							
				TOTAL	17	10	04	24	420	480	900	24
					OR	OR		OR	OR	OR		
					18	08		27	360	540		

e: BSC: Basic Science, PCC: Professional Core, HSMC: Humanity and Social Science, NCMC: Non-credit mandatory course.
KVK39/49 Vyavaharika Kannada (Kannada for communication) is for non-kannada speaking, reading and writing students and 18KAK39/49
dalitha Kannada (Kannada for Administration) is for students who speak, read and write kannada.

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

NCMC	18MATDIP41	Additional Mathematics – II	Mathematics	02	01	--	03	40	60	100	0

The mandatory non – credit courses Additional Mathematics I and II prescribed for III and IV semesters respectively, to the lateral entry Diploma ders admitted to III semester of BE/B.Tech programs, shall attend the classes during the respective semesters to complete all the formalities of the rse and appear for the University examination. In case, any student fails to register for the said course/ fails to secure the minimum 40 % of the scribed CIE marks, he/she shall be deemed to have secured F grade. In such a case, the student have to Fulfill the requirements during subsequent nester/s to appear for SEE.

These Courses shall not be considered for vertical progression, but completion of the courses shall be mandatory for the award of degree.

Courses prescribed to lateral entry B. Sc degree holders admitted to III semester of Engineering programs

teral entrant students from B.Sc. Stream, shall clear the non-credit courses Engineering Graphics and Elements of Civil Engineering and chanics of the First Year Engineering Programme. These Courses shall not be considered for vertical progression, but completion of the courses ll be mandatory for the award of degree.

CTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the uired activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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V SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination			
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks
					L	T	P				
1	HSMC	18ES51	Technological Innovation Management And Entrepreneurship		3	0	--	03	40	60	100
2	PCC	18EC52	Digital Signal Processing		3	2	--	03	40	60	100
3	PCC	18EC53	Principles of Communication Systems		3	2	--	03	40	60	100
4	PCC	18EC54	Information Theory & Coding		3	--	--	03	40	60	100
5	PCC	18EC55	Electromagnetic Waves		3	--	--	03	40	60	100
6	PCC	18EC56	Verilog HDL		3	--	--	03	40	60	100
7	PCC	18ECL57	Digital Signal Processing Laboratory		--	2	2	03	40	60	100
8	PCC	18ECL58	HDL Laboratory		--	2	2	03	40	60	100
9	HSMC	18CIV59	Environmental Studies	Civil/ Environmental [Paper setting: Civil Engineering Board]	1	--	--	02	40	60	100
				TOTAL	19	08	4	26	360	540	900

Note: PCC:Professional Core, HSMC: Humanity and Social Science.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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VI SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC61	Digital Communication		3	2	--	03	40	60	100	4
2	PCC	18EC62	Embedded Systems		3	2	--	03	40	60	100	4
3	PCC	18EC63	Microwave & Antennas		3	2	--	03	40	60	100	4
4	PEC	18XX64X	Professional Elective -1		3	--	--	03	40	60	100	3
5	OEC	18XX65X	Open Elective –A		3	--	--	03	40	60	100	3
6	PCC	18ECL66	Embedded Systems Laboratory		--	2	2	03	40	60	100	2
7	PCC	18ECL67	Communication Laboratory		--	2	2	03	40	60	100	2
8	MP	18ECMP68	Mini-project		--	--	2	03	40	60	100	2
9	Internship	--	Internship	To be carried out during the vacation/s of VI and VII semesters and /or VII and VIII semesters.								
				TOTAL	15	10	6	24	320	480	800	24

Note: PCC: Professional core, PEC: Professional Elective, OE: Open Elective, MP: Mini-project.

Professional Elective -1

Course code under 18XX64X	Course Title
18EC641	Operating System
18EC642	Artificial Neural Networks
18EC643	Object Oriented Programming using C++
18EC644	Digital System Design using Verilog
18EC645	Nanoelectronics

Open Elective –A

(i) 18EC651 Signal Processing (ii)18EC652 Sensors &Signal Conditioning

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX65X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Mini-project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to an individual student or to a group having not more than 4 students.

CIE procedure for Mini-project:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the Mini-project work, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all the guides of the college.

The CIE marks awarded for the Mini-project, shall be based on the evaluation of project report, project presentation skill and question and answer session in the ratio 50:25:25. The marks awarded for the project report shall be the same for all the batch mates.

SEE for Mini-project:

(i) Single discipline: Contribution to the Mini-project and the performance of each group member shall be assessed individually in the semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the Mini-project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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VII SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination			
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks
					L	T	P				
1	PCC	18EC71	Computer Networks		3	--	--	03	40	60	100
2	PCC	18EC72	VLSI Design		3	--	--	03	40	60	100
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100
6	PCC	18ECL76	Computer Networks Lab		--	2	2	03	40	60	100
7	PCC	18ECL77	VLSI Laboratory		--	2	2	03	40	60	100
8	Project	18ECP78	Project Work Phase - 1		--	--	2	--	100	--	100
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)							
				TOTAL	15	4	6	21	380	420	800

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X	Course Title
18EC731	Real Time System
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	Data Structures using C++
18EC735	DSP Algorithms &Architecture

Professional Electives - 3

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning

Open Elective –B

(i) 18EC751 Communication Theory (ii) 18EC752 Neural Networks

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please re the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from diff disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Su Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the co Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skil question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit sha included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not t up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the inter requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning quired activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

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VIII SEMESTER

Sl. No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC81	Wireless and Cellular Communication		3	--	--	03	40	60	100	3
2	PEC	18XX82X	Professional Elective - 4		3	--	--	03	40	60	100	3
3	Project	18ECP83	Project Work Phase - 2		--	--	2	03	40	60	100	8
4	Seminar	18ECS84	Technical Seminar		--	--	2	03	100	--	100	1
5	Internship .	18EC185	Internship	Completed during the vacation/s of VI and VII semesters and /or VII and VIII semesters.)				03	40	60	100	3
				TOTAL	06	--	4	15	260	240	500	18

Note: PCC: Professional Core, PEC: Professional Elective.

Professional Electives - 4

Course code under 18XX82X	Course Title
18EC821	Network Security
18EC822	Micro Electro Mechanical Systems
18EC823	Radar Engineering
18EC824	Optical Communication Networks
18EC825	Biomedical Signal Processing

Project Work

CIE procedure for Project Work Phase - 2:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -2, shall be based on the evaluation of project work phase -2 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

SEE for Project Work Phase - 2:

(i) Single discipline: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted at the department.

(ii) Interdisciplinary: Contribution to the project and the performance of each group member shall be assessed individually in semester end examination (SEE) conducted separately at the departments to which the student/s belong to.

Internship: Those, who have not pursued /completed the internship shall be declared as fail and have to complete during subsequent University examination after satisfying the internship requirements.

AICTE activity Points: In case students fail to earn the prescribed activity Points, Eighth semester Grade Card shall be issued only after earning the required activity Points. Students shall be admitted for the award of degree only after the release of the Eighth semester Grade Card.

Activity points of the students who have earned the prescribed AICTE activity Points shall be sent the University along with the CIE marks of 8th semester. In case of students who have not satisfied the AICTE activity Points at the end of eighth semester, the column under activity Points shall be marked NSAP (Not Satisfied Activity Points).

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BE 2018 SCHEME THIRD SEMESTER SYLLABUS EC / TC

TRANSFORM CALCULUS, FOURIER SERIES AND NUMERICAL TECHNIQUES
(Common to all Branches)
SEMESTER – III (EC / TC)
[As per Choice Based Credit System (CBCS) scheme]

Course Code	18MAT31	CIE Marks	40
Number of Lecture Hours/ Week	02 + 2 (Tutorial)	SEE marks	60
Total Number of LectureHours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Have an insight into Fourier series, Fourier transforms, Laplacetransforms, Difference equations and Z-transforms.
- Develop the proficiency in variational calculus and solving ODE's arising in engineering applications, using numerical methods.

Modules	RBT Level
Module - 1	
Laplace Transform: Definition and Laplace transforms of elementary functions (statements only). Laplace transforms of Periodic functions (statement only) and unit-step function – problems. **Inverse Laplace Transform:** Definition and problems, Convolution theorem to find the inverse Laplace transforms (without Proof) and problems. Solution of linear differential equations using Laplace transforms.	**L1, L2**
Module - 2	
Fourier Series: Periodic functions, Dirichlet's condition. Fourier series of periodic functions period 2π and arbitrary period. Half range Fourier series. Practical harmonic analysis.	**L1, L2**
Module – 3	
Fourier Transforms: Infinite Fourier transforms, Fourier sine and cosine transforms. Inverse Fourier transforms. Problems. **Difference Equations and Z-Transforms:**Difference equations, basic definition, z-transform-definition, Standard z-transforms, Damping and shifting rules, initial value and final value theorems (without proof) and problems, Inverse z-transform and applications to solve difference equations.	**L1, L2**
Module - 4	
Numerical Solutions of Ordinary Differential Equations(ODE's): Numerical solution of ODE's of first order and first degree- Taylor's series method, Modified Euler's method. Runge - Kutta method of fourth order, Milne's and Adam-Bashforth predictor and corrector method (No derivations of formulae)-Problems.	**L1, L2**
Module - 5	

Numerical Solution of Second Order ODE's: Runge-Kutta method and Milne's predictor and corrector method. (No derivations of formulae). **Calculus of Variations:**Variation of function and functional, variational problems, Euler's equation, Geodesics, hanging chain - Problems.	**L1, L2, L3**

Course Outcomes: At the end of the course, the students will be ableto

- Use Laplace transform and inverse Laplace transform in solving differential/ integral equation arising in network analysis, control systems and other fields of engineering.
- Demonstrate Fourier series to study the behaviour of periodic functions and their applications in system communications, digital signal processing and field theory.
- Make use of Fourier transform and Z-transform to illustrate discrete/continuous function arising in wave and heat propagation, signals and systems.
- Solve first and second order ordinary differential equations arising in engineering problems using single step and multistep numerical methods.
- Determine the extremals of functionals using calculus of variations and solve problems arising in dynamics of rigid bodies and vibrational analysis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. E. Kreyszig - Advanced Engineering Mathematics, John Wiley & Sons, 10th Edition, 2016.
2. B.S. Grewal -Higher Engineering Mathematics, Khanna Publishers, 44th Edition, 2017.
3. Srimanta Pal et al - Engineering Mathematics, Oxford University Press, 3rd Edition, 2016.

Reference Books:

1. C.Ray Wylie, Louis C.Barrett - Advanced Engineering Mathematics, McGraw-Hill Book Co, 6th Edition, 1995.
2. S.S.Sastry - Introductory Methods of Numerical Analysis, Prentice Hall of India, 4th Edition 2010.
3. B.V.Ramana - Higher Engineering Mathematics, McGraw-Hill, 11th Edition, 2010.
4. N.P.Bali and Manish Goyal - A Text Book of Engineering Mathematics, LaxmiPublications, 6th Edition, 2014.

B. E. EC / TC
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER - III]

NETWORK THEORY

Subject Code	**18EC32**	CIE Marks	40
Number of Lecture Hours/Week	3:2:0	SEE marks	60
Credits	04	Exam Hours	03

CREDITS – 04

Course Learning Objectives: This course will enable students to:

- Describe basic network concepts emphasizing source transformation, source shifting, mesh and nodal techniques to solve for resistance/impedance, voltage, current and power.
- Explain network Thevenin‘s, Millman‘s, Superposition, Reciprocity, Maximum Power transfer and Norton‘s Theorems and apply them in solving the problems related to Electrical Circuits.
- Explain the behavior of networks subjected to transient conditions.
- Use applications of Laplace transforms to network problems.
- Study two port network parameters like Z, Y, T and h and their inter-relationships and applications

Modules	RBT Level
Module – 1	
Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis with linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh, source transformation.	**L1, L2, L3, L4**
Module – 2	
Network Theorems: Superposition, Reciprocity, Millman‘s theorems, Thevinin‘s and Norton‘s theorems, Maximum Power transfer theorem.	**L1, L2, L3, L4**
Module – 3	
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.	**L1 , L2 , L3**
Module – 4	
Laplace Transformation & Applications: Solution of networks, step, ramp and impulse responses, waveform Synthesis.	**L1, L2, L3, L4**
Module – 5	
Two port network parameters: Definition of Z, Y, h and Transmission parameters, modelling with these parameters, relationship between parameters sets.	**L1, L2, L3, L4**

Course Outcomes: At the end of the course, the students will be ableto

- Determine currents and voltages using source transformation/ source shifting/ mesh/ nodal analysis and reduce given network using star-delta transformation/source transformation/ source shifting.
- Solve network problems by applying Superposition/ Reciprocity/ Thevenin‘s/ Norton‘s/ Maximum Power Transfer/ Millman‘s Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions.
- Calculate current and voltages for the given circuit under transient conditions.
- Apply Laplace transform to solve the given network.
- Solve the given network using specified two port network parameter like Z or Y or Tor h.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. M.E. Van Valkenberg (2000), ―Network analysis‖, Prentice Hall of India, 3rd edition, 2000, ISBN: 9780136110958.
2. Roy Choudhury, ―Networks and systems‖, 2nd edition, New Age InternationalPublications, 2006, ISBN: 9788122427677

Reference Books:

1. Hayt, Kemmerly and Durbin ―Engineering Circuit Analysis‖, TMH 7th Edition,2010.
2. J. David Irwin /R. Mark Nelms, ―Basic Engineering Circuit Analysis‖, John Wiley, 8thed, 2006.
3. Charles K Alexander and Mathew N O Sadiku, ― Fundamentals of Electric Circuits‖, Tata McGraw-Hill, 3rd Ed, 2009.

ELECTRONIC DEVICES
SEMESTER – III (EC / TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC33	CIE Marks	40

Number of LectureHours/Week	03	SEE marks	60
Total Number ofLecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basics of semiconductor physics and electronic devices.
- Describe the mathematical models BJTs and FETs along with the constructional details.
- Understand the construction and working principles of optoelectronic devices
- Understand the fabrication process of semiconductor devices and CMOS process integration.

Module-1	RBT Level
Semiconductors Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. **(Text 1: 3.1.1, 3.1.2, 3.1.3,3.1.4, 3.2.1,3.2.3,3.2.4,3.4.1, 3.4.2,3.4.3,3.4.5).**	**L1,L2**
Module-2	
P-N Junctions Forward and Reverse biased junctions- Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers.**(Text 1: 5.3.1,5.3.3, 5.4, 5.4.1,5.4.2, 5.4.3)** Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials**.(Text 1: 8.1.1, 8.1.2, 8.1.3, 8.2, 8.2.1)**	**L1,L2**
Module – 3	
Bipolar Junction Transistor Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown, Base Resistance and Emitter crowding. **(Text 1: 7.1, 7.2, 7.3, 7.5.1, 7.6, 7.7.1, 7.7.2, 7.7.3, 7.7.5).**	**L1,L2**
Module-4	
Field Effect Transistors Basic pn JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET- Two terminal MOS structure- Energy band diagram, Ideal Capacitance – Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics. **(Text 2: 9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1, 9.8.2).**	**L1,L2**
Module-5	
Fabrication of p-n junctions Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization.**(Text 1: 5.1)** **Integrated Circuits** Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements. **(Text 1:9.1, 9.2, 9.3.1, 9.3.2).**	**L1,L2**
Course outcomes: After studying this course, students will be able to: • Understand the principles of semiconductor Physics • Understand the principles and characteristics of different types of semiconductor devices • Understand the fabrication process of semiconductor devices • Utilize the mathematical models of semiconductor junctions and MOS transistors for circuits and systems.	

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Ben.G.Streetman, Sanjay Kumar Banergee, "Solid State Electronic Devices", 7th Edition, Pearson Education, 2016, ISBN 978-93-325-5508-2.
2. Donald A Neamen, DhrubesBiswas, "Semiconductor Physics and Devices", 4th Edition, MCGraw Hill Education, 2012, ISBN 978-0-07-107010-2.

Reference Book:

1. S.M.Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3rd Edition, Wiley, 2018.
2. A.Bar-Lev, "Semiconductor and Electronic Devices", 3rd Edition, PHI, 1993.

DIGITAL SYSTEM DESIGN
SEMESTER – III (EC/TC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18EC34	CIE Marks	40
Number of LectureHours/Week	03	SIE Marks	60
Total Number ofLecture Hours	40 (08 Hours per Module)	Exam Hour	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine-McClusky Techniques.
- Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators.
- Describe Latches and Flip-flops, Registers and Counters.
- Analyze Mealy and Moore Models.
- Develop state diagrams Synchronous Sequential Circuits.
- Appreciate the applications of digital circuits.

Module – 1	RBT Level
Principles of combinational logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine-McClusky techniques – 3 & 4 variables. **(Text 1 - Chapter 3)**	**L1, L2, L3**

Module – 2	
Analysis and design of combinational logic: Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators.**(Text 1 - Chapter 4).** Programmable Logic Devices, Complex PLD, FPGA. **(Text 3 - Chapter 9, 9.6 to 9.8)**	**L1, L2, L3**
Module -3	
Flip-Flops and its Applications: Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip-flops, Characteristic equations, Registers, binary ripple counters, and synchronous binary counters.**(Text 2 - Chapter 6)**	**L1, L2, L3**
Module -4	
Sequential Circuit Design: Design of a synchronous counter,Design of a synchronous mod-n counter using clockedJK, D, T and SR flip-flops. **(Text 2 - Chapter 6)** Mealy and Moore models, State machine notation, Construction of state diagrams.**(Text 1 - Chapter 6)**	**L1, L2, L3**
Module -5	
Applications of Digital Circuits: Design of a Sequence Detector, Guidelines for construction of state graphs, Design Example – Code Converter, Design of Iterative Circuits (Comparator), Design of Sequential Circuits using ROMs and PLAs,CPLDs and FPGAs, Serial Adder with Accumulator, Design of Binary Multiplier, Design of Binary Divider. **(Text 3 – 14.1, 14.3, 16.2, 16.3, 16.4, 18.1, 18.2, 18.3)**	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain the concept of combinational and sequential logic circuits.
- Design the combinational logic circuits.
- Design the sequential circuits using SR, JK, D, T flip-flops and Mealy & Moore machines
- Design applications of Combinational & Sequential Circuits.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. John M Yarbrough,-Digital Logic Applications and Design, Thomson Learning,2001.
2. Donald D. Givone, ―Digital Principles and Design‖, McGraw Hill, 2002.
3. Charles H Roth Jr., Larry L. Kinney ―Fundamentals of Logic Design, CengageLearning, 7th Edition.

Reference Books:

1. D. P. Kothari and J. S Dhillon, ―Digital Circuits and Design‖, Pearson, 2016,
2. Morris Mano, ―Digital Design‖, Prentice Hall of India, Third Edition.
3. K. A. Navas, ―Electronics Lab Manual‖, Volume I, PHI, 5th Edition, 2015.

COMPUTER ORGANIZATION AND ARCHITECTURE
SEMESTER – III (EC/TC)

[As per Choice Based Credit System (CBCS) Scheme]

CourseCode	**18EC35**	**CIE Marks**	**40**
Numberof Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number ofLectureHours	**40 (08Hours per Module)**	**Exam Hours**	**03**

CREDITS– 03

Course Learning Objectives: This course will enable students to:

- Explain the basic sub systems of a computer, their organization, structure and operation.
- Illustrate the concept of programs as sequences of machine instructions.
- Demonstrate different ways of communicating with I/O devices
- Describe memory hierarchy and concept of virtual memory.
- Illustrate organization of simple pipelined processor and other computing systems.

Module 1	**RBT Level**
Basic Structure of Computers: Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation **(upto 1.6.2 of Chap 1 of Text).** **Machine Instructions and Programs:** Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(upto 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).**	**L1, L2, L3**
Module 2	
Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions **(from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of Text).**	**L1, L2, L3**
Module 3	
Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access**(upto 4.2.4 and 4.4 except 4.4.1 of Chap 4 of Text).**	**L1, L2, L3**
Module 4	
Memory System: Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks **(5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).**	**L1, L2, L3**

Module 5	
Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control **(upto 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain the basic organization of a computer system.
- Explain different ways of accessing an input / output device including interrupts.
- Illustrate the organization of different types of semiconductor and other secondary storage memories.
- Illustrate simple processor organization based on hardwired control and micro programmed control.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.

Reference Books:

1. David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.
2. William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.
3. Vincent P. Heuring& Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

POWER ELECTRONICS AND INSTRUMENTATION
SEMESTER – III (EC/TC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18EC36	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours/ Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Study and analysis of thyristor circuits with different triggering conditions.
- Learn the applications of power devices in controlled rectifiers, converters and inverters.
- Understand types of instrument errors.
- Develop circuits for multirange Ammeters and Voltmeters.
- Describe principle of operation of digital measuring instruments and Bridges.
- Understand the operation of Transducers, Instrumentation amplifiers and PLCs.

Module-1	RBT Level
Introduction: History, Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-OFF mechanisms, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. **(Text 1)**	**L1, L2**
Module-2	
Phase Controlled Converter: Control techniques, Single phase half wave and full wave controlled rectifier with resistive and inductive loads, effect of freewheeling diode. **Choppers:** Chopper Classification, Basic Chopper operation: step-down, step-up and step-up/down choppers. **(Text 1)**	**L1,L2, L3**
Module-3	
Inverters: Classification, Single phase Half bridge and full bridge inverters with RL load. **Switched Mode Power Supplies**: Isolated Flyback Converter, Isolated Forward Converter.(Text 1) **Principles of Measurement:** Static Characteristics, Error in Measurement, Types of Static Error. **(Text 2: 1.2-1.6)** Multirange Ammeters, Multirange voltmeter. **(Text 2: 3.2, 4.4)**	**L1,L2, L3**
Module-4	
Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM **(Text 2: 5.1-5.3, 5.5, 5.6)** **Digital Multimeter:** Digital Frequency Meter and Digital Measurement of Time, Function Generator. **Bridges:** Measurement of resistance: Wheatstone's Bridge, AC Bridges-Capacitance and Inductance Comparison bridge, Wien's bridge. **(Text 2: refer 6.2, 6.3 upto 6.3.2, 6.4 upto 6.4.2, 8.8, 11.2, 11.8-11.10, 11.14).**	**L1, L2**
Module-5	

Transducers: Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT. **(Text 2: 13.1-13.3, 13.5, 13.6 upto 13.6.1, 13.7, 13.8, 13.11).** Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer, Analog Weight Scale **(Text 2: 14.3.3, 14.4.1, 14.4.3).** **Programmable Logic Controller:** Structure, Operation, Relays and Registers **(Text 2: 21.15, 21.15.2, 21.15.3, 21.15.5, 21.15.6).**	**L1,L2, L3**

Course Outcomes: At the end of the course students should be able to:

- Build and test circuits using power electronic devices.
- Analyze and design controlled rectifier, DC to DC converters, DC to AC inverters and SMPS.
- Define instrument errors.
- Develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.
- Describe the principle of operation of Digital instruments and PLCs.
- Use Instrumentation amplifier for measuring physical parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897
2. H. S. Kalsi, "Electronic Instrumentation", McGraw Hill, 3rd Edition, 2012, ISBN: 9780070702066.

Reference Books:

1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.
2. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.
3. David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN 81-203-2360-2.
4. A. D. Helfrick and W.D. Cooper, "Modern Electronic Instrumentation and Measuring Techniques", Pearson, 1st Edition, 2015, ISBN: 9789332556065.

ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY
SEMESTER – III (EC/TC)
[As per Choice Based Credit System (CBCS) scheme]

Laboratory Code	**18ECL37**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This laboratory course enables students to

- Understand the circuit schematic and its working
- Study the characteristics of different electronic devices
- Design and test simple electronic circuits as per the specifications using discrete electronic components.
- Familiarize with EDA software which can be used for electronic circuit simulation.

Laboratory Experiments

PART A : Experiments using Discrete components

1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative)

2. Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor

3. Characteristics of Zener diode and design a Simple Zener voltage regulator determine line and load regulation

4. Characteristics of LDR and Photo diode and turn on an LED using LDR

5. Static characteristics of SCR.

6. SCR Controlled HWR and FWR using RC triggering circuit

7. Conduct an experiment to measure temperature in terms of current/voltage using a temperature sensor bridge.

8. Measurement of Resistance using Wheatstone and Kelvin's bridge.

PART-B : Simulation using EDA software
(EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any equivalent tool)

1. Input and Output characteristics of BJT Common emitter configuration and evaluation of parameters.

2. Transfer and drain characteristics of a JFET and MOSFET.

3. UJT triggering circuit for Controller Rectifiers.

4. Design and simulation of Regulated power supply.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Understand the characteristics of various electronic devices and measurement of parameters.
- Design and test simple electronic circuits
- Use of circuit simulation software for the implementation and characterization of electronic circuits and devices.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-A** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.
2. Muhammed H Rashid, "Introduction to PSpice using OrCAD for circuits and electronics", 3rd Edition, Prentice Hall, 2003.

DIGITAL SYSTEM DESIGN LABORATORY
SEMESTER – III (EC/TC)

[As per Choice Based Credit System (CBCS) Scheme]

Laboratory Code	**18ECL38**	**IA Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**Exam Mark**	**60**
		Exam Hour	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience in design, realization and verification of

- Demorgan'sTheorem,SOP,POSforms
- Full/ParallelAdders,SubtractorsandMagnitudeComparator
- Multiplexer using logicgates
- Demultiplexers andDecoders
- Flip-Flops, Shift registers andCounters.

NOTE: 1. Usediscretecomponentstotestand verifythelogic gates. The IC numbers given are suggestive; any equivalent ICs can beused. 2. For experiment No. 11 and 12 any open source or licensed simulation tool may be used.	**Revised Bloom's Taxonomy (RBT) Level**
Laboratory Experiments:	
1. Verify (i) Demorgan'sTheoremfor2variables. (ii) Thesum-ofproductandproduct-of-sumexpressions using universalgates.	**L1, L2, L3**
2. Design andimplement (i) Half Adder & Full Adder using i) basic gates. ii) NAND gates (ii) Half subtractor& Full subtractor using i) basic gates ii) NAND gates	**L3, L4**

3.Designandimplement (i) 4-bitParallelAdder/Subtractorusing IC 7483. (ii) BCD to Excess-3 code conversion and vice-versa.	**L3, L4**
4. Design and Implementation of (i) 1-bit Comparator (ii) 5-bit Magnitude Comparator using IC 7485.	**L3, L4**
5. Realize (i) Adder &Subtactors using IC 74153. (ii) 4-variable function using IC74151(8:1MUX).	**L2, L3, L4**
6. Realize (i) Adder &Subtractors using IC74139. (ii) Binary to Gray code conversion & vice-versa (74139)	**L2, L3, L4**
7. Realize the following flip-flops using NANDGates. Master-Slave JK, D & T Flip-Flop.	**L2, L3**
8. Realize the following shift registers usingIC7474/7495 (i) SISO (ii) SIPO (iii)) PISO(iv))PIPO (v) Ring (vi) Johnson counter	**L2, L3**
9. Realize (i) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop (ii) Mod-N Counter using IC7490 / 7476 (iii) Synchronous counter using IC74192	**L2, L3**
10. Design Pseudo Random Sequence generator using 7495.	**L2, L3**
11. Design Serial Adder with Accumulator andSimulate using Simulation tool.	**L2, L3, L4**
12. Design Binary Multiplier and Simulate using Simulation tool.	**L2, L3, L4**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Demonstrate the truth table of various expressions and combinational circuits using logicgates.
- Designvarious combinational circuits such asadders, subtractors, comparators, multiplexers anddemultiplexers.
- Construct flips-flops, counters and shiftregisters.
- Simulate Serial adder and Binary Multiplier.

Conduct of PracticalExamination:

- All laboratory experiments are to be includedforpractical examination.
- Students are allowed to pick one experiment from thelot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup ofmarks.
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero.

ADDITIONAL MATHEMATICS – I

(A Bridge course for Lateral Entry students under Diploma quota to BE/B.Techprogrammes)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18MATDIP31**	**CIE Marks**	**40**
Number of Lecture Hours/ Week	**02 + 1 (Tutorial)**	**SEE marks**	**60**
Total Number of LectureHours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 0

Course Learning Objectives: This course will enable students to:

- Provide basic concepts of complex trigonometry, vector algebra, differential and integral calculus.
- Provide an insight into vector differentiation and first order ODE's.

Modules	RBT Level
Module - 1	
Complex Trigonometry: Complex Numbers: Definitions and properties. Modulus and amplitude of a complex number, Argand's diagram, De-Moivre's theorem (without proof). **Vector Algebra:**Scalar and vectors. Addition and subtraction and multiplication of vectors- Dot and Cross products -Problems.	**L1, L2**
Module - 2	
Differential Calculus: Review of successive differentiation-illustrative examples. Maclaurin's series expansions-Illustrative examples. Partial **Differentiation:** Euler's theorem-problems on first order derivatives only. Total derivatives-differentiation of composite functions. Jacobians of order two-Problems.	**L1, L2**
Module – 3	
Vector Differentiation: Differentiation of vector functions. Velocity and acceleration of a particle moving on a space curve. Scalar and vector point functions. Gradient, Divergence, Curl-simple problems. Solenoidal and irrotational vector fields-Problems.	**L1, L2**
Module - 4	
Integral Calculus: Review of elementary integral calculus. Reduction formulae for sinnx, cosnx (with proof) and sinmxcosnx (without proof) and evaluation of these with standard limits-Examples. Double and triple integrals-Simple examples.	**L1, L2**
Module - 5	
Ordinary differential equations (ODE's). Introduction-solutions of first order and first degree differential equations: exact, linear differential equations. Equations reducible to exact and Bernoulli's equation.	**L1, L2**

Course Outcomes: At the end of the course, the students will be ableto

- CO1: Apply concepts of complex numbers and vector algebra to analyze the problems arising in related area.
- CO2: Use derivatives and partial derivatives to calculate rate of change of multivariate functions.
- CO3: Analyze position, velocity and acceleration in two and three dimensions of vector valued functions.
- CO4: Learn techniques of integration including the evaluation of double and triple integrals.
- CO5: Identify and solve first order ordinary differential equations.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. B.S. Grewal - Higher Engineering Mathematics, Khanna Publishers, 43rd Edition, 2015.

Reference Books:

1. E. Kreyszig - Advanced Engineering Mathematics, John Wiley & Sons, 10th Edition, 2015.
2. N.P.Bali and Manish Goyal - Engineering Mathematics, Laxmi Publishers, 7th Edition, 2007.
3. RohitKhurana - Engineering Mathematics Vol.I, Cengage Learning, 1st Edition, 2015.

CONSTITUTION of INDIA, PROFESSIONAL ETHICS and CYBER LAW (CPC)
(Common to all Branches)
[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18CPC39/49**	**CIE Marks**	**40**

Number of Lecture Hours/ Week	02(Tutorial)	SEE marks	60
		Exam Hours	03

CREDITS – 01

Course Learning Objectives: This course will enable students to:

- To know the fundamental political codes, structure, procedures, powers, and duties of Indian government institutions, fundamental rights, directive principles, and the duties of citizens
- To understand engineering ethics and their responsibilities, identify their individual roles and ethical responsibilities towards society.
- To know about the cybercrimes and cyber laws for cyber safety measures.

Modules	RBT Level
Module - 1	
Introduction to Indian Constitution: The Necessity of the Constitution, The Societies before and after the Constitution adoption.Introduction to the Indian constitution, The Making of the Constitution, The Role of the Constituent Assembly - Preamble and Salient features of the Constitution of India. Fundamental Rights and its Restriction and limitations in different Complex Situations. Directive Principles of State Policy (DPSP) and its present relevance in our society with examples. Fundamental Duties and its Scope and significance in Nation building.	**L1, L2, L3**
Module - 2	
Union Executive and State Executive: Parliamentary System, Federal System, Centre-State Relations. Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies.Supreme Court of India, Judicial Reviews and Judicial Activism.State Executives – Governor, Chief Minister, State Cabinet, State Legislature, High Court and Subordinate Courts, Special Provisions (Articles 370.371,371J) for some States.	**L1, L2, L3**
Module – 3	
Elections, Amendmentsand Emergency Provisions: Elections, Electoral Process, and Election Commission of India, Election Laws. Amendments - Methods in Constitutional Amendments (How and Why) and Important Constitutional Amendments. Amendments – 7,9,10,12,42,44, 61, 73,74, ,75, 86, and 91,94,95,100,101,118 and some important Case Studies. Emergency Provisions, types of Emergencies and its consequences. **Constitutional special provisions:** Special Provisions for SC and ST, OBC, Women, Children and Backward Classes.	**L1, L2, L3**
Module - 4	
Professional / Engineering Ethics: Scope & Aims of Engineering & Professional Ethics - Business Ethics, Corporate Ethics, Personal Ethics. Engineering and Professionalism, Positive and Negative Faces of Engineering Ethics, Code of Ethics as defined in the website of Institutionof Engineers (India): Profession, Professionalism, and ProfessionalResponsibility. Clash of Ethics, Conflicts of Interest.Responsibilities in Engineering Responsibilities in Engineering and Engineering Standards, the impediments to Responsibility.Trust and Reliability in Engineering, IPRs (Intellectual Property Rights), Risks, Safety and liability in Engineering.	**L1, L2, L3**
Module - 5	
Internet Laws, Cyber Crimes and Cyber Laws: Internet and Need for Cyber Laws, Modes of Regulation of Internet, Types of cyber terror capability, Net neutrality, Types of Cyber Crimes, India and cyber law, Cyber Crimes and the information Technology Act 2000, Internet Censorship.Cybercrimes and enforcement agencies.	**L1, L2, L3**

Course Outcomes: At the end of the course, the students will be ableto

- Have constitutional knowledge and legal literacy.
- Understand Engineering and Professional ethics and responsibilities of Engineers.
- Understand the cybercrimes and cyber laws for cyber safety measures.

Question paper pattern:

- The SEE question paper will be set for 100 marks and the marks scored by the students will proportionately be reduced to 60. The pattern of the question paper will be objective type (MCQ).
- For the award of 40 CIE marks, refer the University regulations 2018.

Text Books:

1. Shubham Singles, Charles E. Haries, and et al: "Constitution of India, Professional Ethics and Human Rights" byCengage Learning India, Latest Edition – 2019.
2. Alfred Basta and et al: "Cyber Security and Cyber Laws"byCengage Learning India - 2018. Chapter – 19, Page No's: 359 to 383.

Reference Books:

1. Durga Das Basu (DD Basu): "Introduction to the Constitution of India", (Students Edition.) Prentice –Hall, 2008.
2. M.Govindarajan, S.Natarajan, V.S.Senthilkumar, "Engineering Ethics", Prentice – Hall, 2004.

COMPLEX ANALYSIS, PROBABILITY AND STATISTICAL METHODS
SEMESTER – IV (EC/TC)
[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18MAT41**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**2+2 (Tutorial)**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Provide an insight into applications of complex variables, conformal mapping and special functions arising in potential theory, quantum mechanics, heat conduction and field theory.
- Develop probability distribution of discrete, continuous random variables and joint probability distribution occurring in digital signal processing, design engineering and microwave engineering.

Modules	**RBT Level**
Module -1	
Calculus of complex functions: Review of function of a complex variable, limits, continuity, and differentiability. Analytic functions: Cauchy-Riemann equations in cartesian and polar forms and consequences. Construction of analytic functions: Milne-Thomson method-Problems.	**L1, L2**
Module -2	
Conformal transformations: Introduction. Discussion oftransformations: $w=z^2$, $w=e^z$, $w=z+\frac{1}{z},(z\neq 0)$. Bilinear transformations- Problems. **Complex integration:** Line integral of a complex function-Cauchy's theorem and Cauchy's integral formula and problems.	**L1, L2**
Module -3	
Probability Distributions: Review of basic probability theory. Random variables (discrete andcontinuous), probability mass/density functions. Binomial, Poisson, exponential and normaldistributions- problems (No derivation for mean and standard deviation)-Illustrative examples.	**L1, L2, L3**
Module -4	
Curve Fitting: Curve fitting by the method of least squares- fitting the curves of the form- $y=ax+b, y=ax^b$ & $y=ax^2+bx+c.$ **Statistical Methods:** Correlation and regression-Karl Pearson's coefficient of correlation and rank correlation-problems. Regression analysis- lines of regression – problems.	**L1,L2, L3**
Module -5	

Joint probability distribution: Joint Probability distribution for two discrete random variables, expectation and covariance. **Sampling Theory:** Introduction to sampling distributions, standard error, Type-I and Type-II errors. Test of hypothesis for means, student's t-distribution, Chi-square distribution as a test of goodness of fit.	**L2, L3, l4**

Course Outcomes: At the end of this course students will demonstrate the ability to

- Use the concepts of analytic function and complex potentials to solve the problems arising in electromagnetic field theory.
- Utilize conformal transformation and complex integral arising in aerofoil theory, fluid flow visualization and image processing.
- Apply discrete and continuous probability distributions in analyzing the probability models arising in engineering field.
- Make use of the correlation and regression analysis to fit a suitable mathematical model for the statistical data.
- Construct joint probability distributions and demonstrate the validity of testing the hypothesis.

Question paper pattern:

1. Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
2. Each full question can have a maximum of 4 sub questions.
3. There will be 2 full questions from each module covering all the topics of the module.
4. Students will have to answer 5 full questions, selecting one full question from each module.
5. The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Advanced Engineering Mathematics, E. Kreyszig, John Wiley & Sons, 10th Edition, 2016.
2. Higher Engineering Mathematics, B.S. Grewal, Khanna Publishers, 44th Edition, 2017.
3. Engineering Mathematics, Srimanta Pal et al, Oxford University Press, 3rd Edition, 2016.

Reference Books:

1. Advanced Engineering Mathematics, C.Ray Wylie, Louis C.Barrett, McGraw-Hill, 6th Edition 1995.
2. Introductory Methods of Numerical Analysis, S.S.Sastry, Prentice Hall of India, 4th Edition 2010.
3. Higher Engineering Mathematics, B.V.Ramana, McGraw-Hill, 11th Edition, 2010.
4. A Text Book of Engineering Mathematics, N.P.Bali and Manish Goyal, Laxmi Publications, 6th Edition, 2014.

ANALOG CIRCUITS
SEMESTER – IV (EC/TC)
[As per Choice Based Credit System (CBCS) scheme]

Subject Code	**18EC42**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3+2 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course Learning Objectives: This course will enable students to:

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing, and demonstrate the use of FET amplifiers.
- Construct frequency response of FET amplifiers at various frequencies.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Modules	**RBT Level**
Module -1	
BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor. **Small signal operation and Models**: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model. **MOSFETs: Biasing in MOS amplifier circuits:** Fixing V_{GS}, Fixing V_G, Drain to Gate feedback resistor. **Small signal operation and modeling**: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance.	**L1, L2,L3**

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.6), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.6)]	
Module -2	
MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance $R_{S,}$ Source follower. **MOSFET internal capacitances and High frequency model:** The gate capacitive effect, Junction capacitances, High frequency model. **Frequency response of the CS amplifier**: The three frequency bands, high frequency response, Low frequency response. **Oscillators:** FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) **[Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]**	**L1, L2, L3**
Module -3	
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages,, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. **[Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]**	**L1, L2, L3**
Module -4	
Op-Amp with Negative Feedback and general applications Inverting and Non inverting Amplifiers – Closed Loop voltage gain, Input impedance, Output impedance, Bandwidth with feedback. DC and AC Amplifiers, Summing, Scaling and Averaging Amplifiers, Instrumentation amplifier, Comparators, Zero Crossing Detector, Schmitt trigger. **[Text 2: 3.3(3.3.1 to 3.3.6), 3.4(3.4.1 to 3.4.5) 6.2, 6.5, 6.6 (6.6.1), 8.2, 8.3, 8.4]**	**L1,L2, L3**
Module -5	
Op-Amp Circuits: DAC - Weighted resistor and R-2R ladder, ADC- Successive approximation type, Small Signal half wave rectifier, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and AstableMultivibrators. **[Text 2: 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2, 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]**	**L1, L2, L3**

Course Outcomes: At the end of this course students will demonstrate the ability to

- Understand the characteristics of BJTs and FETs.
- Design and analyze BJT and FET amplifier circuits.
- Design sinusoidal and non-sinusoidal oscillators.
- Understand the functioning of linear ICs.
- Design of Linear IC based circuits.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford, 2015.ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition. Pearson Education, 2000. ISBN: 8120320581

Reference Books:

1. Electronic Devices and Circuit Theory, Robert L Boylestad and Louis Nashelsky, 11th Edition, Pearson Education, 2013, ISBN: 978-93-325-4260-0.
2. Fundamentals of Microelectronics, BehzadRazavi, 2nd Edition, John Weily, 2015, ISBN 978-81-265-7135-2
3. J.Millman&C.C.Halkias—Integrated Electronics, 2nd edition, 2010, TMH. ISBN 0-07-462245-5

CONTROL SYSTEMS
SEMESTER – IV (EC / TC)
[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC43**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basic features, configurations andapplication of control systems.
- Understand various terminologies and definitions for the control systems.
- Learn how to find a mathematical model of electrical, mechanical and electro-mechanicalsystems.
- Know how to fin d time response from the transfer function.
- Find the transfer function via Mason s' rule.
- Analyze the stability of a system from the transfer function.

Modules	**RBT Level**
Module – 1	
Introduction to Control Systems: Types of Control Systems, Effect of Feedback System s, Differential equation of Physical Systems –Mechanical Systems, Electrical Systems, Electromechanical systems, Analogous Systems.	**L1, L2, L3**
Module – 2	
Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs.	**L1, L2, L3**
Module – 3	
Time Response of feedback controlsystems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design).	**L1, L2, L3**
Module – 4	
Stability analysis: Concepts of stability, Necessary conditions forStability, Routhstability criterion, Relative stability analysis: more on the Routh stability criterion. Introduction to Root-Locus Techniques, The root locus concepts, Construction of rootloci. **Frequencydomain analysis and stability:**Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function.	**L1, L2, L3**
Module – 5	
Introduction to Polar Plots, (Inverse Polar Plots excluded) Mathematical preliminaries, NyquistStability criterion, (System s with transportation lag excluded) Introduction to lead, lag and lead- lag compensating networks (excluding design). **Introduction to State variable analysis:** Concepts ofstate, state variable and state models for electrical systems, Solution of state equations.	**L1, L2, L3**

Course Outcomes: Atthe end of the course, the students will be ableto

- Develop the mathematical model of mechanical and electrical systems.
- Develop transfer function for a given control system using blockdiagram reduction techniques and signal flow graph method.
- Determine the time domain specification s for first an d second order systems.
- Deter mine the stability of a system in the time domain using Routh-Hurwitz criterion and Root-locus technique.
- Determine the s stability of a system in the frequency domain u sing Nyquistand bodeplots.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

J. Nagarath an d M.Gopal, " Control System s Engineering", New Age International(P) Limited, Publishers, Fifthedition- 2005,ISBN: 81 - 224 - 2008-7.

Reference Books:

1. "Modern Control Engineering," K.Ogata, Pearson Education Asia/ PHI,4th Edition, 2002. ISBN 978 - 81 - 203 - 4010 - 7.
2. "Automatic Control Systems", Benjamin C. Kuo, JohnWiley India Pvt. Ltd.,8th Edition, 2008.
3. "Feedback and Control System," Joseph J Distefano III et al., Schaum'sOutlines, TMH, 2nd Edition 2007.

ENGINEERING STATISTICS and LINEAR ALGEBRA SEMESTER – IV (EC/TC) [As per Choice Based Credit System (CBCS) Scheme]			
Course Code	**18EC44**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number ofLecture Hours	**40 (8 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand and Analyze Single and Multiple Random Variables, and their extension to Random Processes.
- Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications.
- Compute the quantitative parameters for functions of single and Multiple Random Variables and Processes.
- Compute the quantitative parameters for Matrices and Linear Transformations.

Module-1	**RBT Level**
Single Random Variables: Definition of random variables, cumulative distribution function continuous and discrete random variables; probability mass function, probability density functions and properties; Expectations, Characteristic functions, Functions of single Random Variables, Conditioned Random variables. Application exercises to Some special distributions: Uniform, Exponential, Laplace, Gaussian; Binomial, and Poisson distribution. **(Chapter 4 Text 1)**	**L1, L2, L3**
Module -2	
Multiple Random variables: Concept, Two variable CDF and PDF, Two Variable expectations (Correlation, orthogonality, Independent), Two variable transformation, Two Gaussian Random variables, Sum of two independent Random Variables, Sum of IID Random Variables – Central limit Theorem and law of large numbers, Conditional joint Probabilities, Application exercises to Chi-square RV, Student-T RV, Cauchy and Rayleigh RVs. **(Chapter 5 Text 1)**	**L1, L2, L3**
Module-3	
Random Processes: Ensemble, PDF, Independence, Expectations, Stationarity, Correlation Functions (ACF, CCF, Addition, and Multiplication), Ergodic Random Processes, Power Spectral Densities (Wiener Khinchin, Addition and Multiplication of RPs, Cross spectral densities), Linear Systems (output Mean, Cross correlation and Auto correlation of Input and output), Exercises with Noise. **(Chapter 6 Text 1)**	**L1, L2, L3**
Module -4	
Vector Spaces: Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations **Orthogonality:** Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram- Schmidt Orthogonalization procedure. **(Refer Chapters 2 and 3 Text 2)**	**L1, L2, L3**
Module -5	
Determinants: Properties of Determinants, Permutations and Cofactors. **(Refer Chapter 4, Text 2**) **Eigenvalues and Eigen vectors:** Review of Eigenvalues and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. **(Refer Chapter 5, Text 2)**	**L1, L2, L3**

Course outcomes: After studying this course, students will be able to:

- Identify and associate Random Variables and Random Processes in Communication events.
- Analyze and model the Random events in typical communication events to extract quantitative statistical parameters.
- Analyze and model typical signal sets in terms of a basis function set of Amplitude, phase and

frequency.

- Demonstrate by way of simulation or emulation the ease of analysis employing basis functions, statistical representation and Eigenvalues.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Richard H Williams, "Probability, Statistics and Random Processes for Engineers" Cengage Learning, 1st Edition, 2003, ISBN 13: 978-0-534- 36888-3, ISBN 10: 0-534-36888-3.
2. Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327

Reference Books:

1. Hwei P. Hsu, "Theory and Problems of Probability, Random Variables, and Random Processes" Schaums Outline Series, McGraw Hill. ISBN 10: 0-07- 030644-3.
2. K. N. HariBhat, K AnithaSheela, JayantGanguly, "Probability Theory and Stochastic Processes for Engineers", Cengage Learning India, 2019, ISBN: Not in book

SIGNALS AND SYSTEMS
SEMESTER – IV (EC/TC)
[As per Choice Based Credit System (CBCS)

Course Code	**18EC45**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number ofLecture Hours	**40 (8 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the mathematical description of continuous and discrete time signals and systems.
- Analyze the signals in time domain using convolution sum and Integral.
- Classify signals into different categories based on their properties.
- Analyze Linear Time Invariant (LTI) systems in time and transform domains.

Module-1	**RBT Level**

Introduction and Classification of signals: Definition of signal and systems, communication and control system as examples Classification of signals. **Basic Operations on signals**: Amplitude scaling, addition, multiplication, differentiation, integration, time scaling, time shift and time reversal. **Elementary signals/Functions**: Exponential, sinusoidal, step,impulse and ramp functions. Expression of triangular, rectangular and other waveforms in terms of elementary signals.	**L1, L2, L3**
Module -2	
System Classification and properties: Linear-nonlinear, Time variant-invariant, causal-noncausal,static-dynamic, stable-unstable, invertible. **Time domain representation of LTI System:** Impulse response, convolution sum, convolution integral. Computation of convolution sum and convolution integral using graphical method for unit step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular.	**L1, L2, L3**
Module-3	
LTI system Properties in terms of impulse response: System interconnection,Memoryless,Causal,Stable,InvertibleandDeconvolution, and step response. **Fourier Representation of Periodic Signals**: CTFSproperties and basic problems.	**L1, L2, L3**
Module -4	
Fourier Representation of aperiodic Signals: Introduction to Fourier Transform & DTFT, Definition and basic problems. **Properties of Fourier Transform**: Linearity, Time shift, Frequency shift, Scaling, Differentiation and Integration, Convolution and Modulation, Parseval's theorem and problems on properties of Fourier Transform.	**L1, L2, L3**
Module -5	
The Z-Transforms: Z transform, properties of the region of convergence, properties of the Z-transform, Inverse Z-transform, Causality and stability, Transform analysis of LTI systems.	**L1, L2, L3**

Course Outcomes: At the end of the course, students will be able to:

- Analyze the different types of signals and systems.
- Determine the linearity, causality, time-invariance and stability properties of continuous and discrete time systems.
- Represent continuous and discrete systems in time and frequency domain using different transforms Test whether the system is stable.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Simon Haykins and Barry Van Veen, "Signals and Systems", 2nd Edition, 2008, Wiley India. ISBN 9971-51-239-4.

Reference Books:

1. **Michael Roberts,** "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN 978-0-07-070221-9.
2. **Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab,** "Signals and Systems" Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002.
3. **H.P Hsu, R. Ranjan,** "Signals and Systems", Scham's outlines, TMH, 2006.
4. **B. P. Lathi,** "Linear Systems and Signals", Oxford University Press, 2005.
5. **Ganesh Rao and SatishTunga,** "Signals and Systems", Pearson/Sanguine.

MICROCONTROLLER
IV Semester (EC/TC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18EC46**	**CIE Marks**	**40**
Number of LectureHours/Week	**03**	**SEE Marks**	**60**
Total Number ofLecture Hours	**40 (8 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the difference between a Microprocessor and a Microcontroller and embedded microcontrollers.
- Familiarize the basic architecture of 8051 microcontroller.
- Program 8051microprocessor using Assembly Level Language and C.
- Understand the interrupt system of 8051 and the use of interrupts.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051.
- Interface 8051 to external memory and I/O devices using its I/O ports.

Module-1	**RBT Level**
8051 Microcontroller: Microprocessor Vs Microcontroller, Embedded Systems, Embedded Microcontrollers, 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing.	**L1, L2**

Module -2

8051 Instruction Set: Addressing Modes, Data Transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Bit manipulation instructions. Simple Assembly language program examples (without loops) to use these instructions.	**L1, L2**
Module-3	
8051 Stack, I/O Port Interfacing and Programming: 8051 Stack, Stack and Subroutine instructions. Assembly language program examples on subroutine and involving loops. Interfacing simple switch and LED to I/O ports to switch on/off LED with respect to switch status.	**L1, L2, L3**
Module -4	
8051 Timers and Serial Port: 8051 Timers and Counters – Operation and Assembly language programming to generate a pulse using Mode-1 and a square wave using Mode-2 on a port pin. 8051 Serial Communication- Basics of Serial Data Communication, RS-232 standard, 9 pin RS232 signals, Simple Serial Port programming in Assembly and C to transmit a message and to receive data serially.	**L1, L2, L3**
Module -5	
8051 Interrupts and Interfacing Applications: 8051 Interrupts. 8051 Assembly language programming to generate an external interrupt using a switch, 8051 C programming to generate a square waveform on a port pin using a Timer interrupt. Interfacing 8051 to ADC-0804, DAC, LCD and Stepper motor and their 8051 Assembly language interfacing programming.	**L1, L2, L3**

Course outcomes: At the end of the course, students will be able to:

- Explain the difference between Microprocessors & Microcontrollers, Architecture of 8051 Microcontroller, Interfacing of 8051 to external memory and Instruction set of 8051.
- Write 8051 Assembly level programs using 8051 instruction set.
- Explain the Interrupt system, operation of Timers/Counters and Serial port of 8051.
- Write 8051 Assembly language program to generate timings and waveforms using 8051 timers, to send & receive serial data using 8051 serial port and to generate an external interrupt using a switch.
- Write 8051 Assembly language programs to generate square wave on 8051 I/O port pin using interrupt and C Programme to send & receive serial data using 8051 serial port.
- Interface simple switches, simple LEDs, ADC 0804, LCD and Stepper Motor to 8051 using 8051 I/O ports.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "The 8051 Microcontroller and Embedded Systems – using assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006.

2. "The 8051 Microcontroller", Kenneth J. Ayala, 3rd Edition, Thomson/Cengage Learning.

Reference Books:

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

MICROCONTROLLER LABORATORY **SEMESTER – IV(EC/TC)** **[As per Choice Based Credit System (CBCS) scheme]**			
Laboratory Code	**18ECL47**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**
CREDITS – 02			

Course Learning Objectives: This laboratory course enables students to

- Understand the basics of microcontroller and its applications.
- Have in-depth knowledge of 8051 assembly language programming.
- Understand controlling the devices using C programming.
- The concepts of I/O interfacing for developing real time embedded systems.

Laboratory Experiments

I. PROGRAMMING

1. Data Transfer: Block Move, Exchange, Sorting, Finding largest element in an array.
2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.
7. Programs to generate delay, Programs using serial port and on-Chip timer/counter.

II. INTERFACING

1. Interface a simple toggle switch to 8051 and write an ALP to generate an interrupt which switches on an LED (i) continuously as long as switch is on and (ii) only once for a small time when the switch is turned on.
2. Write a C program to (i) transmit and (ii) to receive a set of characters serially by interfacing 8051 to a terminal.
3. Write ALPs to generate waveforms using ADC interface.
4. Write ALP to interface an LCD display and to display a message on it.
5. Write ALP to interface a Stepper Motor to 8051 to rotate the motor.
6. Write ALP to interface ADC-0804 and convert an analog input connected to it.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Write Assembly language programs in 8051 for solving simple problems that manipulate input data using different instructions of 8051.
- Interface different input and output devices to 8051 and control them using Assembly language programs.
- Interface the serial devices to 8051 and do the serial transfer using C programming.

Conduct of PracticalExamination:

- All laboratory experiments are to be includedforpractical examination.
- Students are allowed to pick one experiment from thelot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup ofmarks.
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero.

ANALOG CIRCUITS LABORATORY
SEMESTER – IV (EC/TC)
[As per Choice Based Credit System (CBCS) scheme]

Laboratory Code	**18ECL48**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This laboratory course enables students to

- Understand the circuit configurations and connectivity of BJT and FET Amplifiers and Study of frequency response
- Design and test of analog circuits using OPAMPs
- Understand the feedback configurations of transistor and OPAMP circuits
- Use of circuit simulation for the analysis of electronic circuits.

Laboratory Experiments

PART A : Hardware Experiments

1. Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.
2. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
3. Design and set-up BJT/FET i) Colpitts Oscillator, and ii) Crystal Oscillator
4. Design active second order Butterworth low pass and high pass filters.
5. Design Adder, Integrator and Differentiator circuits using Op-Amp
6. Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.
7. Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
8. Design Monostable and AstableMultivibrator using 555 Timer.

PART-B : Simulation using EDA software (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any other equivalent tool can be used)

1. RC Phase shift oscillator and Hartley oscillator
2. Narrow Band-pass Filter and Narrow band-reject filter
3. Precision Half and full wave rectifier
4. Monostable and AstableMultivibrator using 555 Timer.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Design analog circuits using BJT/FETs and evaluate their performance characteristics.
- Design analog circuits using OPAMPs for different applications
- Simulate and analyze analog circuits that usesICs for different electronic applications.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.

ADDITIONAL MATHEMATICS – II

(A Bridge course for Lateral Entry students under Diploma quota to BE/B.Techprogrammes)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18MATDIP41**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**2+1 (Tutorial)**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 0			

Course Learning Objectives: This course will enable students to:

- Provide essential concepts of linear algebra, second & higher order differential equations along with methods to solve them.
- Provide an insight into elementary probability theory and numerical methods.

Modules	**RBT Level**
Module -1	
Linear Algebra: Introduction - rank of matrix by elementary row operations - Echelon form. Consistency of system of linear equations - Gauss elimination method. Eigen values and eigen vectors of a square matrix. Problems.	**L1, L2**
Module -2	
Numerical Methods: Finite differences. Interpolation/extrapolation using Newton's forward and backward difference formulae (Statements only)-problems. Solution of polynomial and transcendental equations – Newton-Raphson and Regula-Falsi methods (only formulae)- Illustrative examples. Numerical integration: Simpson's one third rule and Weddle's rule (without proof) Problems.	**L1, L2, L3**
Module -3	
Higher order ODE's: Linear differential equations of second and higher order equations with constant coefficients. Homogeneous /non-homogeneous equations. Inverse differential operators.[Particular Integral restricted to R(x)= e^{ax}, $\sin ax$ /$\cos ax$ for $f(D)y = R(x)$.]	**L1, L2**
Module -4	
Partial Differential Equations (PDE's): Formation of PDE's by elimination of arbitrary constants and functions. Solution of non-homogeneous PDE by direct integration. Homogeneous PDEs involving derivative with respect to one independent variable only.	**L1,L2**
Module -5	
Probability: Introduction. Sample space and events. Axioms of probability. Addition & multiplication theorems. Conditional probability, Bayes's theorem, problems.	**L1,L2**

Course Outcomes: At the end of this course students will demonstrate the ability to

- Solve systems of linear equations using matrix algebra.
- Apply the knowledge of numerical methods in modelling and solving engineering problems.
- Make use of analytical methods to solve higher order differential equations.
- Classify partial differential equations and solve them by exact methods.
- Apply elementary probability theory and solve related problems.

Question paper pattern:

1. Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
2. Each full question can have a maximum of 4 sub questions.
3. There will be 2 full questions from each module covering all the topics of the module.
4. Students will have to answer 5 full questions, selecting one full question from each module.
5. The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Higher Engineering Mathematics, B.S. Grewal, Khanna Publishers, 43rd Edition, 2015.

Reference Books:

1. Advanced Engineering Mathematics, E. Kreyszig, John Wiley & Sons, 10th Edition, 2015.
2. Engineering Mathematics, N.P.Bali and Manish Goyal, Laxmi Publishers, 7th Edition, 2007.
3. Engineering Mathematics Vol.I, RohitKhurana, Cengage Learning, 1st Edition, 2015.

CONSTITUTION OF INDIA, PROFESSIONAL ETHICS AND CYBER LAW (CPC)

(Common to all Branches)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18CPC39/49**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02(Tutorial)**	**SEE marks**	**60**
		Exam Hours	**03**

CREDITS – 01

Course Learning Objectives: This course will enable students to:

- To know the fundamental political codes, structure, procedures, powers, and duties of Indian government institutions, fundamental rights, directive principles, and the duties of citizens
- To understand engineering ethics and their responsibilities, identify their individual roles and ethical responsibilities towards society.
- To know about the cybercrimes and cyber laws for cyber safety measures.

Modules	RBT Level
Module - 1	

Introduction to Indian Constitution: The Necessity of the Constitution, The Societies before and after the Constitution adoption. Introduction to the Indian constitution, The Making of the Constitution, The Role of the Constituent Assembly - Preamble and Salient features of the Constitution of India. Fundamental Rights and its Restriction and limitations in different Complex Situations. Directive Principles of State Policy (DPSP) and its present relevance in our society with examples. Fundamental Duties and its Scope and significance in Nation building.	**L1, L2, L3**
Module - 2	
Union Executive and State Executive: Parliamentary System, Federal System, Centre-State Relations. Union Executive – President, Prime Minister, Union Cabinet, Parliament - LS and RS, Parliamentary Committees, Important Parliamentary Terminologies. Supreme Court of India, Judicial Reviews and Judicial Activism. State Executives – Governor, Chief Minister, State Cabinet, State Legislature, High Court and Subordinate Courts, Special Provisions (Articles 370.371,371J) for some States.	**L1, L2, L3**
Module – 3	
Elections, Amendments and Emergency Provisions: Elections, Electoral Process, and Election Commission of India, Election Laws. Amendments - Methods in Constitutional Amendments (How and Why) and Important Constitutional Amendments. Amendments – 7,9,10,12,42,44, 61, 73,74, ,75, 86, and 91,94,95,100,101,118 and some important Case Studies. Emergency Provisions, types of Emergencies and its consequences. **Constitutional special provisions:** Special Provisions for SC and ST, OBC, Women, Children and Backward Classes.	**L1, L2, L3**
Module - 4	
Professional / Engineering Ethics: Scope & Aims of Engineering & Professional Ethics - Business Ethics, Corporate Ethics, Personal Ethics. Engineering and Professionalism, Positive and Negative Faces of Engineering Ethics, Code of Ethics as defined in the website of Institution of Engineers (India): Profession, Professionalism, and Professional Responsibility. Clash of Ethics, Conflicts of Interest. Responsibilities in Engineering Responsibilities in Engineering and Engineering Standards, the impediments to Responsibility. Trust and Reliability in Engineering, IPRs (Intellectual Property Rights), Risks, Safety and liability in Engineering.	**L1, L2, L3**
Module - 5	
Internet Laws, Cyber Crimes and Cyber Laws: Internet and Need for Cyber Laws, Modes of Regulation of Internet, Types of cyber terror capability, Net neutrality, Types of Cyber Crimes, India and cyber law, Cyber Crimes and the information Technology Act 2000, Internet Censorship. Cybercrimes and enforcement agencies.	**L1, L2, L3**
Course Outcomes: At the end of the course, the students will be ableto • Have constitutional knowledge and legal literacy. • Understand Engineering and Professional ethics and responsibilities of Engineers. • Understand the cybercrimes and cyber laws for cyber safety measures.	
Question paper pattern: • The SEE question paper will be set for 100 marks and the marks scored by the students will proportionately be reduced to 60. The pattern of the question paper will be objective type (MCQ). • For the award of 40 CIE marks, refer the University regulations 2018.	

Text Books:

1. Shubham Singles, Charles E. Haries, and et al: “Constitution of India, Professional Ethics and Human Rights” byCengage Learning India, Latest Edition – 2019.
2. Alfred Basta and et al: “Cyber Security and Cyber Laws”byCengage Learning India - 2018. Chapter – 19, Page No’s: 359 to 383.

Reference Books:

1. Durga Das Basu (DD Basu): “Introduction to the Constitution of India”, (Students Edition.) Prentice –Hall, 2008.
2. M.Govindarajan, S.Natarajan, V.S.Senthilkumar, “Engineering Ethics”, Prentice –Hall, 2004.

TECHNOLOGICAL INNOVATION MANAGEMENT AND ENTREPRENEURSHIP
SEMESTER – V (EC/TC/EI/BM/ML)
[As per Choice Based Credit System (CBCS) Scheme

Course Code	**18ES51**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand basic skills of Management
- Understand the need for Entrepreneurs and their skills
- Identify the Management functions and Social responsibilities
- Understand the Ideation Process, creation of Business Model, Feasibility Study and sources of funding

Module-1	**RBT Level**
Management: Nature and Functions of Management – Importance, Definition, Management Functions, Levels of Management, Roles of Manager, Managerial Skills, Management & Administration, Management as a Science, Art &**Profession (Selected topics of Chapter 1, Text 1).** **Planning:** Planning-Nature, Importance, Types, Steps and Limitations of Planning; Decision Making – Meaning, Types and Steps in Decision Making(**Selected topics from Chapters 4 & 5, Text 1).**	**L1,L2**
Module-2	
Organizing and Staffing: Organization-Meaning, Characteristics, Process of Organizing, Principles of Organizing, Span of Management (meaning and importance only), Departmentalisation, Committees–Meaning, Types of Committees; Centralization Vs Decentralization of Authority and Responsibility; **Staffing**-Need and Importance**,** Recruitment and Selection Process **(Selected topics from Chapters 7, 8 & 11,Text 1).** **Directing and Controlling:** Meaning and Requirements of Effective Direction, Giving Orders; Motivation-Nature of Motivation, Motivation Theories (Maslow's Need-Hierarchy Theory and Herzberg's Two Factor Theory); Communication – Meaning, Importance and Purposes of Communication; Leadership-Meaning, Characteristics, Behavioural Approach of Leadership; Coordination-Meaning, Types, Techniques of Coordination; Controlling – Meaning, Need for Control System, Benefits of Control, Essentials of Effective Control System, Steps in Control Process (**Selected topics from Chapters 15 to 18 and 9, Text 1).**	**L1,L2**
Module-3	
Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance **(Selected topics from Chapter 3, Text 1).** **Entrepreneurship**: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship **(Selected topics from Chapter 2, Text 2).**	**L1,L2**
Module-4	
Family Business: Role and Importance of Family Business, Contributions of Family Business in India, Stages of Development of a Family Business, Characteristics of a Family-owned Business in India, Various types of family businesses **(Selected topics from Chapter 4,(Page 71-75) Text 2).** **Idea Generation and Feasibility Analysis-** Idea Generation; Creativity and Innovation; Identification of Business Opportunities; Market Entry Strategies; Marketing Feasibility; Financial Feasibilities; Political Feasibilities; Economic Feasibility; Social and Legal Feasibilities; Technical Feasibilities; Managerial Feasibility, Location and Other Utilities Feasibilities.**(Selected topics from Chapter 6(Page No. 111-117) & Chapter 7(Page No. 140-142), Text 2)**	**L1,L2**
Module-5	

Business model – Meaning, designing, analyzing and improvising; Business Plan – Meaning, Scope and Need; Financial, Marketing, Human Resource and Production/Service Plan; Business plan Formats; Project report preparation and presentation; Why some Business Plan fails? **(Selected topics from Chapter 8 (Page No 159-164, Text 2)** **Financing and How to start a Business?** Financial opportunity identification; Banking sources; Nonbanking Institutions and Agencies; Venture Capital – Meaning and Role in Entrepreneurship; Government Schemes for funding business; Pre launch, Launch and Post launch requirements; Procedure for getting License and Registration; Challenges and Difficulties in Starting an Enterprise**(Selected topics from Chapter 7(Page No 147-149), Chapter 5(Page No 93-99) & Chapter 8(Page No. 166-172) Text 2)** **Project Design and Network Analysis:** Introduction, Importance of Network Analysis, Origin of PERT and CPM, Network, Network Techniques, Need for Network Techniques, Steps in PERT, CPM, Advantages, Limitations and Differences**.(Selected topics from Chapters 20, Text 3).**	**L1,L2,L 3**

Course Outcomes: After studying this course, students will be able to:

- Understand the fundamental concepts of Management and Entrepreneurship and opportunities in order to setup a business
- Describe the functions of Managers, Entrepreneurs and their social responsibilities
- Understand the components in developing a business plan
- Awareness about various sources of funding and institutions supporting entrepreneurs

Text Books:

1. Principles of Management – P.C Tripathi, P.N Reddy, McGraw Hill Education, 6th Edition, 2017. ISBN-13:978-93-5260-535-4.
2. Entrepreneurship Development Small Business Enterprises- Poornima M Charantimath, Pearson Education 2008, ISBN 978-81-7758-260-4.
3. Dynamics of Entrepreneurial Development and Management by Vasant Desai. HPH 2007, ISBN: 978-81-8488-801-2.
4. Robert D. Hisrich, Mathew J. Manimala, Michael P Peters and Dean A. Shepherd, "Entrepreneurship", 8th Edition, Tata Mc-graw Hill Publishing Co.ltd.-new Delhi, 2012

Reference Book:

1. Essentials of Management: An International, Innovation and Leadership perspective by Harold Koontz, Heinz Weihrich McGraw Hill Education, 10th Edition 2016. ISBN- 978-93-392-2286-4.

DIGITAL SIGNAL PROCESSING

V Semester(EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC52**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3+2(Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course Learning Objectives: This course will enable students to

- Understand the frequency domain sampling and reconstruction of discrete time signals.
- Study the properties and the development of efficient algorithms for the computation of DFT.
- Realization of FIR and IIR filters in different structural forms.
- Learn the procedures to design of IIR filters from the analog filters using impulse invariance and bilinear transformation.
- Study the different windows used in the design of FIR filters and design appropriate filters based on the specifications.
- Understand the architecture and working of DSP processor

Module-1	**RBT Level**
Discrete Fourier Transforms (DFT): Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution, Additional DFT properties. **[Text 1]**	**L1,L2, L3**
Module-2	
Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences. **Fast-Fourier-Transform (FFT) algorithms:** Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT–decimation-in-time and decimation-in-frequency algorithms. **[Text 1]**	**L1,L2, L3**
Module-3	
Design of FIR Filters: Characteristics of practical frequency –selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures**.[Text1]**	**L1,2,L3**
Module-4	
IIR Filter Design: Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Lowpass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth Filter Design using BLT. Realization of IIR Filters in Direct form I and II. **[Text 2]**	**L1,L2,L3**
Module-5	
Digital Signal Processors: DSP Architecture, DSP Hardware Units, Fixed point format, Floating point Format, IEEE Floating point formats, Fixed point digital signal processors, Floating point processors, FIR and IIR filter implementations in Fixed point systems**.[Text 2]**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Determine response of LTI systems using time domain and DFT techniques.
- Compute DFT of real and complex discrete time signals.
- Computation of DFT using FFT algorithms and linear filtering approach.
- Design and realize FIR and IIR digital filters
- Understand the DSP processor architecture.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60

Text Book:

1. Proakis&Monalakis, "Digital signal processing – Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9.
2. Li Tan, Jean Jiang, "Digital Signal processing – Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.

Reference Books:

1. Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition, McGraw Hill Education, 2013,
2. Oppenheim & Schaffer, "Discrete Time Signal Processing" , PHI, 2003.
3. D.GaneshRao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231

PRINCIPLES OF COMMUNICATION SYSTEMS

V Semester (EC/TC)

[**As per Choice Based Credit System (CBCS) scheme]**

Subject Code	**18EC53**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3+2 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**

CREDITS – 04

Course Learning Objectives: This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM., Low pass sampling and Quantization as a random process.
- Understand and analyse concepts digitization of signals viz; sampling, quantizing and encoding.
- Evolve the concept of SNR in the presence of channel induced noise and study Demodulation of analog modulated signals.
- Evolve the concept of quantization noise for sampled and encoded signals and study the concepts of reconstruction from these samples at a receiver.

Module-1	RBT Level
AMPLITUDE MODULATION: Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector. **(3.1 – 3.2 in Text)** **DOUBLE SIDE BAND-SUPPRESSED CARRIER MODULATION:** Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **(3.3 – 3.4 in Text)** **SINGLE SIDE–BAND AND VESTIGIAL SIDEBAND METHODS OF MODULATION:** SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing,Theme Example: VSB Transmission of Analog and Digital Television. **(3.5 – 3.8 in Text)**	**L1, L2, L3**
Module-2	
ANGLE MODULATION: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems. The SuperheterodyneReceiver **(4.1 – 4.6 of Text)**	**L1, L2,L3**
Module-3	
[Review of Mean, Correlation and Covariance functions of Random Processes. ***(No questions to be set on these topics)]*** **NOISE** - Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth **(5.10 in Text)** **NOISE IN ANALOG MODULATION:** Introduction, Receiver Model, Noise in DSB-SC receivers. Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM **(6.1 – 6.6 in Text)**	**L1, L2,L3**
Module-4	
SAMPLING AND QUANTIZATION: Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation. Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves.**(7.1 – 7.7 in Text)**	**L1, L2,L3**
Module-5	
SAMPLING AND QUANTIZATION (Contd): The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing; Delta Modulation **(7.8 – 7.10 in Text)**, Application examples - (a) Video + MPEG **(7.11 in Text)** and (b) Vocoders**(refer Section 6.8 of Reference Book 1)**.	**L1, L2,L3**

Course Outcomes: After studying this course, students will be able to:

- Analyze and compute performance of AM and FM modulation in the presence of noise at the receiver.
- Analyze and compute performance of digital formatting processes with quantization noise.
- Multiplex digitally formatted signals at Transmitter and demultiplex the signals and reconstruct digitally formatted signals at the receiver.
- Design/Demonstrate the use of digital formatting in Multiplexers, Vocoders and Video transmission.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"Communication Systems", Simon Haykins&Moher, 5th Edition, John Willey, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Books:

1. Modern Digital and Analog Communication Systems, B. P. Lathi, Oxford University Press., 4th edition.
2. An Introduction to Analog and Digital Communication, Simon Haykins, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.
3. Principles of Communication Systems, H.Taub&D.L.Schilling, TMH,2011.
4. CommunicationSystems, Harold P.E, Stern Samy and A.Mahmond, Pearson Edition, 2004.

INFORMATION THEORY and CODING
V Semester (EC/TC)
[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC54**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to

- Understand the concept of Entropy, Rate of information and order of the source with reference to dependent and independent source.
- Study various source encoding algorithms.
- Model discrete & continuous communication channels.
- Study various error control coding algorithms.

Module-1	**RBT Level**
Information Theory: Introduction, Measure of information, Information content of message, Average Information content of symbols in Long Independent sequences, Average Information content of symbols in Long dependent sequences, Markov Statistical Model for Information Sources, Entropy and Information rate of Markoff Sources **(Section 4.1, 4.2 of Text 1)**	**L1, L2,L3**
Module-2	
Source Coding: Encoding of the Source Output, Shannon's Encoding Algorithm**(Sections 4.3, 4.3.1 of Text 1),** Shannon Fano Encoding Algorithm **(Section 2.15 of Reference Book 4)** Source coding theorem, Prefix Codes, Kraft McMillan Inequality property – KMI, Huffman codes **(Section 2.2 of Text 2)**	**L1, L2,L3**
Module-3	
Information Channels: Communication Channels, Discrete Communication channels Channel Matrix, Joint probabilty Matrix, Binary Symmetric Channel, System Entropies. **(Section 4.4, 4.5,**	**L1, L2, L3**

4.51,4.5.2 of Text 1) Mutual Information, Channel Capacity, Channel Capacity of Binary Symmetric Channel, **(Section 2.5, 2.6 of Text 2)** Binary Erasure Channel, Muroga,s Theorem **(Section 2.27, 2.28 of Reference Book 4)**	
Module-4	
Error Control Coding: Introduction, Examples of Error control coding, methods of Controlling Errors, Types of Errors, types of Codes, Linear Block Codes: matrix description of Linear Block Codes, Error detection & Correction capabilities of Linear Block Codes, Single error correction Hamming code, Table lookup Decoding using Standard Array. **Binary Cyclic Codes:** Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit Shift register, Syndrome Calculation, Error Detection and Correction **(Sections 9.1, 9.2,9.3,9.3.1,9.3.2,9.3.3 of Text 1)**	**L1, L2, L3**
Module-5	
Convolution Codes: Convolution Encoder, Time domain approach, Transform domain approach, Code Tree, Trellis and State Diagram, The Viterbi Algorithm) **(Section 8.5 – Articles 1,2 and 3, 8.6- Article 1 of Text 2)**	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain concept of Dependent & Independent Source, measure of information, Entropy, Rate of Information and Order of a source
- Represent the information using Shannon Encoding, Shannon Fano, Prefix and Huffman Encoding Algorithms
- Model the continuous and discrete communication channels using input, output and joint probabilities
- Determine a codeword comprising of the check bits computed using Linear Block codes, cyclic codes & convolutional codes
- Design the encoding and decoding circuits for Linear Block codes, cyclic codes, convolutional codes, BCH and Golay codes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Digital and analog communication systems, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. Digital communication, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

Reference Books:

1. ITC and Cryptography, Ranjan Bose, TMH, II edition, 2007
2. Principles of digital communication, J. Das, S. K. Mullick, P. K. Chatterjee, Wiley, 1986 - Technology & Engineering
3. Digital Communications – Fundamentals and Applications, Bernard Sklar, Second Edition, Pearson Education, 2016, ISBN: 9780134724058.
4. Information Theory and Coding, HariBhat, Ganesh Rao, Cengage, 2017.
5. Error Correction Coding by Todd K Moon,Wiley Std. Edition, 2006

ELECTROMAGNETIC WAVES
V Semester (EC/TC)
[As per Choice Based Credit System (CBCS)

Course Code	**18EC55**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient.
- Understand the applications of Coulomb‘s law and Gauss law to different charge distributions and the applications of Laplace‘s and Poisson‘s Equations to solve real time problems on capacitance of different charge distributions.
- Understand the physical significance of Biot-Savart‘s, Amperes‘s Law and Stokes‘theorem for different current distributions.
- Infer the effects of magnetic forces, materials and inductance.
- Know the physical interpretation of Maxwell‘ equations and applications for Plane waves for their behavior in different media.
- Acquire knowledge of Poynting theorem and its application of power flow.

Module-1	**RBT Level**
Revision of Vector Calculus – **(Text 1: Chapter 1)** **Coulomb's Law, Electric Field Intensity and Flux density**: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems. **(Text: Chapter 2.1 to 2.5, 3.1)**	**L1, L2, L3**
Module -2	
Gauss's law and Divergence: Gauss 'law, Application of Gauss' law to point charge, line charge, Surface charge and volume charge, Point (differential) form of Gauss law, Divergence. Maxwell‘s First equation (Electrostatics), Vector Operator ▼ and divergence theorem, Numerical Problems (**Text: Chapter 3.2 to 3.7).** **Energy, Potential and Conductors**: Energy expended or work done in moving a point charge in an electric field, The line integral, Definition of potential difference and potential, The potential field of point charge, Potential gradient, Numerical Problems **(Text: Chapter 4.1 to 4.4 and 4.6).**Current and Current density, Continuity of current. **(Text: Chapter 5.1, 5.2)**	**L1, L2, L3**
Module-3	
Poisson's and Laplace's Equations: Derivation of Poisson‘s and Laplace‘s Equations, Uniqueness theorem, Examples of the solution of Laplace‘s equation, Numerical problems on Laplace equation **(Text: Chapter 7.1 to 7.3)** **Steady Magnetic Field**: Biot-Savart Law, Ampere‘s circuital law, Curl, Stokes‘ theorem, Magnetic flux and magnetic flux density, Basic concepts Scalar and Vector Magnetic Potentials, Numerical problems. (**Text: Chapter 8.1 to 8.6)**	**L1, L2, L3**
Module -4	
Magnetic Forces: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3).** **Magnetic Materials**: Magnetization and permeability, Magnetic boundary conditions, The magnetic circuit, Potential energy and forces on magnetic materials, Inductance and mutual reactance, Numerical problems **(Text: Chapter 9.6 to 9.7).** Faraday' law of Electromagnetic Induction –Integral form and Point form,Numerical problems **(Text: Chapter 10.1)**	**L1, L2, L3**
Module -5	
Maxwell's equations Continuity equation, Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell‘s equations in point form, and integral form, Maxwell's equations for different media, Numerical problems **(Text: Chapter 10.2 to 10.4)** **Uniform Plane Wave**: Plane wave, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Solution of wave equation for perfect dielectric, Relation between E and H, Wave propagation in free space, Solution of wave equation for sinusoidal excitation, wave propagation in any conducting media (**γ, α, β, η**) and good conductors, Skin effect or Depth of penetration, Poynting‘s theorem and wave power, Numerical problems. **(Text: Chapter 12.1 to 12.4)**	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
- Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.
- Determine potential and energy with respect to point charge and capacitance using Laplace equation

and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations
- Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
- Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

W.H. Hayt and J.A. Buck, ―Engineering Electromagnetics‖, 8th Edition, Tata McGraw-Hill, 2014, ISBN-978-93-392-0327-6.

Reference Books:

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford university press, 4th Edn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balman, PHI, 2nd Edn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
   N. NarayanaRao, ―Fundamentals of Electromagnetics for Engineering‖, Pearson.

Verilog HDL
V Semester (EC/TC)

[Asper Choice Based credit System (CBCS) Scheme}

CourseCode	**18EC56**	**IA Marks**	**40**
Numberof Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of LectureHours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS– 03

CourseObjectives:
- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks, Functions and Directives.
- Understand timing and delay Simulation.
- Understand the concept of logic synthesis and its impact in verification

Module 1	**RBT Level**
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. **Hierarchical Modeling Concepts:** Top-down and bottom-up design methodology, differences	**L1,L2,L3**

between modules and module instances, parts of a simulation, design block, stimulus block.	
Module 2	
Basic Concepts: Lexical conventions, data types, system tasks, compiler directives. **Modules and Ports:** Module definition, port declaration, connecting ports, hierarchical name referencing.	**L1,L2,L3**
Module 3	
Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. **Dataflow Modeling:** Continuous assignments, delay specification, expressions, operators, operands, operator types.	**L1,L2,L3**
Module 4	
Behavioral Modeling: Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks. **Tasks and Functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions.	**L1,L2,L3**
Module 5	
Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks. **Logic Synthesis with Verilog:**Logic Synthesis, Impact of logic synthesis, Verilog HDL Synthesis, Synthesis design flow, Verification of Gate-Level Netlist**. (Chapter 14 till 14.5 of Text).**	**L1,L2,L3**

Course Outcomes: At the end of this course, students should be able to

- Write Verilog programs in gate, dataflow (RTL), behavioral and switch modeling levels of Abstraction.
- Design and verify the functionality of digital circuit/system using test benches.
- Identify the suitable Abstraction level for a particular digital design.
- Write the programs more effectively using Verilog tasks, functions and directives.
- Perform timing and delay Simulation
- Interpret the various constructs in logic synthesis.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Samir Palnitkar, "**Verilog HDL: A Guide to Digital Design and Synthesis"**, Pearson Education, Second Edition.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier.

DIGITAL SIGNAL PROCESSING LABORATORY

B.E., V Semester, EC/TC

[As per Choice Based Credit System (CBCS) scheme]

CourseCode	**18ECL57**	**IA Marks**	**40**

Numberof LectureHours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**Exam marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS– 02

Course Learning Objectives: This course will enable students to

- Simulate discrete time signals and verification of sampling theorem.
- Compute the DFT for a discrete signal and verification of its properties using MATLAB.
- Find solution to the difference equations and computation of convolution and correlation along with the verification of properties.

1. Compute and display the filtering operations and compare with the theoretical values.
2. Implement the DSP computations on DSP hardware and verify the result.

Laboratory Experiments

Following Experiments to be done using MATLAB / SCILAB / OCTAVE or equivalent:

1. Verification of sampling theorem (use interpolation function).
2. Linear and circular convolution of two given sequences, Commutative, distributive and associative property of convolution.
3. Auto and cross correlation of two sequences and verification of their properties
4. Solving a given difference equation.
5. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum (using DFT equation and verify it by built-in routine).
6. (i) Verification of DFT properties (like Linearity and Parseval's theorem, etc.)
   (ii) DFT computation of square pulse and Sinc function etc.
7. Design and implementation of Low pass and High pass FIR filter to meet the desired specifications (using different window techniques) and test the filter with an audio file. Plot the spectrum of audio signal before and after filtering.
8. Design and implementation of a digital IIR filter (Low pass and High pass) to meet given specifications and test with an audio file. Plot the spectrum of audio signal before and after filtering.

Following Experiments to be done using DSP kit

9. Obtain the Linear convolution of two sequences.
10. Compute Circular convolution of two sequences.
11. Compute the N-point DFT of a given sequence.
12. Determine the Impulse response of first order and second order system.
13. Generation of Sine wave and standard test signals

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Understand the concepts of analog to digital conversion of signals and frequency domain sampling of signals.
- Modeling of discrete time signals and systems and verification of its properties and results.
- Implementation of discrete computations using DSP processor and verify the results.
- Realize the digital filters using a simulation tool and analyze the response of the filter for an audio signal.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
3. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. Vinay K Ingle, John G Proakis, Digital Signal Processing using MATLAB, Fourth Edition, Cengage India Private Limited, 2017.

HDL LABORATORY

V Semester, EC/TC

[As per Choice Based Credit System (CBCS) scheme]

Laboratory Code	**18ECL58**	**CIEMarks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions)+ 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Familiarize with the CAD tool to write HDL programs.
- Understand simulation and synthesis of digital design.
- Program FPGAs/CPLDs to synthesize the digital designs.
- Interface hardware to programmable ICs through I/O ports.
- Choose either Verilog or VHDL for a given Abstraction level.

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD board and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

Laboratory Experiments

PART A : Programming

1. Write Verilog program for the following combinational design along with test bench to verify the design:
    a. 2 to 4 decoder realization using NAND gates only (structural model)
    b. 8 to 3 encoder with priority and without priority (behavioural model)
    c. 8 to 1 multiplexer using case statement and if statements
    d. 4-bit binary to gray converter using 1-bit gray to binary converter 1-bit adder and subtractor

2. Model in Verilog for a full adder and addfunctionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the modeled behaviour.

3. Verilog 32-bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is presented in Table 1.
    a. Write test bench to verify the functionality of the ALU considering all possible input patterns
    b. The enable signal will set the output to required functions if enabled, if disabled all the outputs are set to tri-state
    c. The acknowledge signal is set high after every operation is completed

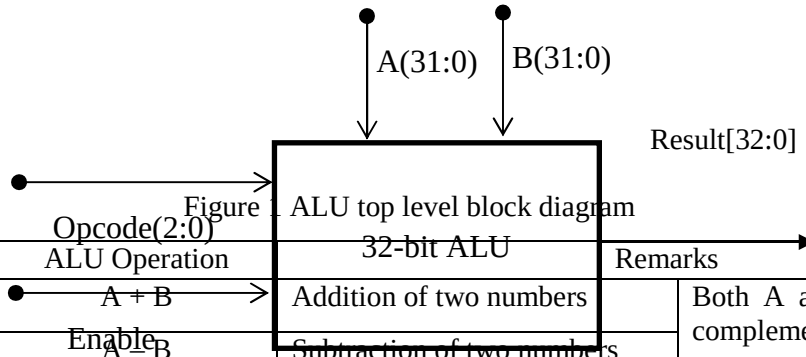

Figure 1 ALU top level block diagram

Opcode(2:0)	ALU Operation		Remarks
000	A + B	Addition of two numbers	Both A and B are in two's complement format
001	A – B	Subtraction of two numbers	
010	A + 1	Increment Accumulator by 1	A is in two's complement format
011	A - 1	Decrement accumulator by 1	
100	A	True	Inputs can be in any format
101	A Complement	Complement	
110	A OR B	Logical OR	
111	A AND B	Logical AND	

Table 1 ALU Functions

4. Write Verilog code for SR, D and JK and verify the flip flop.

5. Write Verilog code for 4-bit BCD synchronous counter.

6. Write Verilog code for counter with given input clock and check whether it works asclock divider performing division of clock by 2, 4, 8 and 16. Verify the functionality of the code.

PART-B : Interfacing and Debugging (EDWinXP, PSpice, MultiSim, Proteus, CircuitLab or any other equivalent tool can be used)

1. Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rd and 1/4thclock from a given input clock. Port the design to FPGA and validate the functionality through oscilloscope.

2. Interface a DC motor to FPGA and write Verilog code to change its speed and direction.

2

3. Interface a Stepper motor to FPGA and write Verilog code to control the Stepper motor rotation which in turn may control a Robotic Arm. External switches to be used for different controls like rotate the Stepper motor (i) +N steps if Switch no.1 of a Dip switch is closed (ii) +N/2 steps if Switch no. 2 of a Dip switch is closed (iii) –N steps if Switch no. 3 of a Dip switch is closed etc.

4. Interface a DAC to FPGA and write Verilog code to generate Sine wave of frequency F KHz (eg. 200 KHz) frequency. Modify the code to down sample the frequency to F/2 KHz. Display the Original and Down sampled signals by connecting them to an oscilloscope.

5. Write Verilog code using FSM to simulate elevator operation.

6. Write Verilog code to convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs, 7-segment display digits or LCD display.

Course Outcomes: At the end of this course, students should be able to:

- Write the Verilog/VHDL programs to simulate Combinational circuits in Dataflow, Behavioral and Gate level Abstractions.
- Describe sequential circuits like flip flops and counters in Behavioral description and obtain simulation waveforms.
- Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.
- Interface the hardware to the programmable chips and obtain the required output.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

ENVIRONMENTAL STUDIES
V Semester – Common to all Branches
[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18CIV59**	**CIE Marks**	**40**
Teaching Hours / Week (L:T:P)	**(1:0:0)**	**SEE Marks**	**60**
Credits	**01**	**Exam Hours**	**02**
Revised Bloom's Taxonomy Levels	L_1- Remembering, L_2 – Understanding.		

Module - 1

Ecosystems (Structure and Function): Forest, Desert, Wetlands, Riverine, Oceanic and Lake. 02 Hrs
Biodiversity: Types, Value; Hot-spots; Threats and Conservation of biodiversity, Forest Wealth, and Deforestation. 02 Hrs

Module - 2

Advances in Energy Systems(Merits, Demerits, Global Status and Applications)**:** Hydrogen, Solar, OTEC, Tidal and Wind. 02 Hrs
Natural Resource Management (Concept and case-studies): Disaster Management, Sustainable Mining, Cloud Seeding, and Carbon Trading.02 Hrs

Module - 3

Environmental Pollution (Sources, Impacts, Corrective and Preventive measures, Relevant Environmental Acts, Case-studies)**:** Surface and Ground Water Pollution; Noise pollution; Soil Pollution and Air Pollution.02 Hrs
Waste Management & Public Health Aspects: Bio-medical Wastes; Solid waste; Hazardous wastes; E-wastes; Industrial and Municipal Sludge. 02 Hrs

Module - 4

Global Environmental Concerns(Concept, policies and case-studies):Ground water depletion/recharging, Climate Change; Acid Rain; Ozone Depletion; Radon and Fluoride problem in drinking water; Resettlement and rehabilitation of people, Environmental Toxicology. 04 Hrs

Module - 5

Latest Developments in Environmental Pollution Mitigation Tools (Concept and Applications): G.I.S. & Remote Sensing,Environment Impact Assessment, Environmental Management Systems, ISO14001; Environmental Stewardship- NGOs. 03 Hrs
Field work: Visit to anEnvironmental Engineering Laboratory or Green Building or Water Treatment Plant or Waste water treatment Plant; ought to be Followed by understanding of process and its brief documentation. 01 Hr

Course outcomes: At the end of the course, students will be able to:

- Understand the principles of ecology and environmental issues that apply to air, land, and water issues on a global scale,
- Develop critical thinking and/or observation skills, and apply them to the analysis of a problem or question related to the environment.
- Demonstrate ecology knowledge of a complex relationship between biotic and a biotic components.
- Apply their ecological knowledge to illustrate and graph a problem and describe the realities that managers face when dealing with complex issues.

Question paper pattern:

- The Question paper will have 100 objective questions.
- Each question will be for 01 marks
- Student will have to answer all the questions in an OMR Sheet.
- The Duration of Exam will be 2 hours.

Sl. No.	Title of the Book	Name of the Author/s	Name of the Publisher	Edition and Year

Textbook/s				
1	Environmental Studies	Benny Joseph	Tata McGraw – Hill.	2nd Edition, 2012
2	Environmental Studies	S M Prakash	Pristine Publishing House, Mangalore	3rd Edition, 2018
3	Environmental Studies – From Crisis to Cure	R Rajagopalan	Oxford Publisher	2005
Reference Books				
1	Principals of Environmental Science and Engineering	Raman Sivakumar	Cengage learning, Singapur.	2nd Edition, 2005
2	Environmental Science – working with the Earth	G.Tyler Miller Jr.	Thomson Brooks /Cole,	11th Edition, 2006
3	Text Book of Environmental and Ecology	Pratiba Sing, AnoopSingh& PiyushMalaviya	Acme Learning Pvt. Ltd. New Delhi.	1st Edition

BE 2018 Scheme Sixth Semester EC Syllabus

DIGITAL COMMUNICATION

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18EC61	CIE Marks	40
Number of LectureHours/Week	03 + 02 (Tutorial)	SEE Marks	60
		Exam Hours	03

CREDITS – 04

Course Learning Objectives: This course will enable students to:

- Understand the mathematical representation of signal, symbol, and noise.
- Understand the concept of signal processing of digital data and signal conversion to symbols at the transmitter and receiver.
- Compute performance metrics and parameters for symbol processing and recovery in ideal and corrupted channel conditions.
- Compute performance parameters and mitigate channel induced impediments in corrupted channel conditions.

Module-1	RBT Level
Bandpass Signal to Equivalent Low pass: Hilbert Transform, Pre-envelopes, Complex envelopes, Canonical representation of bandpass signals, Complex low pass representation of bandpass systems, Complex representation of band pass signals and systems **(Text 1: 2.8, 2.9, 2.10, 2.11, 2.12, 2.13).** **Line codes:** Unipolar, Polar, Bipolar (AMI) and Manchester code and their power spectral densities **(Text 1: Ch 6.10).** Overview of HDB3, B3ZS, B6ZS **(Ref. 1: 7.2)**	**L1,L2,L3**
Module-2	
Signaling over AWGN Channels- Introduction, Geometric representation of signals, Gram-Schmidt Orthogonalization procedure, Conversion of the continuous AWGN channel into a vector channel, Optimum receivers using coherent detection: ML Decoding, Correlation receiver, matched filter receiver **(Text 1: 7.1, 7.2, 7.3, 7.4).**	**L1,L2,L3**
Module – 3	
Digital Modulation Techniques: Phase shift Keying techniques using coherent detection: generation, detection and error probabilities of BPSK and QPSK, M–ary PSK, M–ary QAM **(Relevant topics in Text 1 of 7.6, 7.7).** Frequency shift keying techniques using Coherent detection: BFSK generation, detection and error probability **(Relevant topics in Text 1 of 7.8).** Non coherent orthogonal modulation techniques: BFSK, DPSK Symbol representation, Block diagrams treatment of Transmitter and Receiver, Probability of error (without derivationof probability of error equation) **(Text 1: 7.11, 7.12. 7.13).**	**L1,L2,L3**
Module-4	
Communication through Band Limited Channels: Digital Transmission through Band limited channels: Digital PAM Transmission through Band limited Channels, Signal design for Band limited Channels: Design of band limited signals for zero ISI–The Nyquist Criterion (statement only), Design of band limited signals with controlled ISI-Partial Response signals, Probability of error for detection of Digital PAM: Probability of error for detection of Digital PAM with Zero ISI, Symbol–by–Symbol detection of data with controlled ISI **(Text 2: 9.1, 9.2, 9.3.1, 9.3.2).** Channel Equalization: Linear Equalizers (ZFE, MMSE), **(Text 2: 9.4.2).**	**L1,L2,L3**
Module-5	
Principles of Spread Spectrum: Spread Spectrum Communication Systems: Model of a Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Systems, Effect of De-spreading on a narrowband Interference, Probability of error (statement only), Some applications of DS Spread Spectrum Signals, Generation of PN Sequences, Frequency Hopped Spread Spectrum, CDMA based on IS-95 **(Text 2: 11.3.1, 11.3.2, 11.3.3, 11.3.4, 11.3.5, 11.4.2).**	**L1,L2,L3**
Course Outcomes: At the end of the course, the students will be able to: • Associate and apply the concepts of Bandpass sampling to well specified signals and channels. • Analyze and compute performance parameters and transfer rates for low pass and bandpass symbol under ideal and corrupted non band limited channels. • Test and validate symbol processing and performance parameters at the receiver under	

ideal and corrupted bandlimited channels.
- Demonstrate that bandpass signals subjected to corruption and distortion in a bandlimited channel can be processed at the receiver to meet specified performance criteria.

Question paper pattern:
- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Simon Haykin, "Digital Communication Systems", John Wiley & sons, First Edition, 2014, ISBN 978-0-471-64735-5.
2. John G Proakis and MasoudSalehi, "Fundamentals of Communication Systems", 2014 Edition, Pearson Education, ISBN 978-8-131-70573-5.

Reference Books:

1. B.P.Lathi and Zhi Ding, "Modern Digital and Analog communication Systems", Oxford University Press, 4th Edition, 2010, ISBN: 978-0-198-07380-2.
2. Ian A Glover and Peter M Grant, "Digital Communications", Pearson Education, Third Edition, 2010, ISBN 978-0-273-71830-7.
3. Bernard Sklar and Ray, "Digital Communications - Fundamentals and Applications", Pearson Education, Third Edition, 2014, ISBN: 978-81-317-2092-9.

EMBEDDED SYSTEMS
SEMESTER – VI (EC/TC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18EC62**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03+2 (Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course Learning Objectives: This course will enable students to:

- Explain the architectural features and instructions of 32 bit microcontroller -ARM Cortex M3.
- Develop Programs using the various instructions of ARM Cortex M3 and C language for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Module 1	RBT Level
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, Debugging support, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence **(Text 1: Ch-1, 2, 3)**	**L1,L2**
Module 2	
ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming **(Text 1: Ch-4, Ch-10.1 to 10.6)**	**L1,L2, L3**
Module 3	
Embedded System Components: Embedded Vs General computing system, Classification of Embedded systems, Major applications and purpose of ES. Elements of an Embedded System (Block diagram and explanation), Differences between RISC and CISC, Harvard and Princeton, Big and Little Endian formats, Memory (ROM and RAM types), Sensors, Actuators, Optocoupler, Communication Interfaces (I2C, SPI, IrDA, Bluetooth, Wi-Fi, Zigbee only) **(Text 2: All the Topics from Ch-1 and Ch-2 (Fig and explanation before 2.1) 2.1.1.6 to 2.1.1.8, 2.2 to 2.2.2.3, 2.3 to 2.3.2, 2.3.3.3, selected topics of 2.4.1 and 2.4.2 only)**.	**L1,L2**
Module 4	
Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language). **Text 2: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)**	**L1,L2, L3**
Module 5	

RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques **(Text 2: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Ch-12, Ch-13 (a block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)**	**L1,L2, L3**

Course outcomes: After studying this course, students will be able to:

- Describe the architectural features and instructions of 32 bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Develop the hardwaresoftware co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", 2nd Edition, Newnes, (Elsevier), 2010.
2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2nd Edition.

Reference Books:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008, ISBN: 978-0-471-72180-2.
2. Yifeng Zhu, "Embedded Systems with Arm Cortex-M Microcontrollers in Assembly Language and C", 2nd E -Man Press LLC ©2015 ISBN:0982692633 9780982692639.
3. Embedded real time systems by K.V. K. K Prasad, Dreamtech publications, 2003.
4. Embedded Systems by Rajkamal, 2nd Edition, McGraw hill Publications, 2010.

MICROWAVE and ANTENNAS
SEMESTER – VI EC
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18EC63**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03+02(Tutorial)**	**SEE Marks**	**60**
		Exam Hours	**03**
CREDITS – 04			

Course Learning Objectives: This course will enable students to:

- Describe the microwave properties and its transmission media
- Describe microwave devices for several applications
- Understand the basics of antenna theory
- Select antennas for specific applications

Module 1	**RBT Level**

Microwave Tubes: Introduction, Reflex Klystron Oscillator, Mechanism of Oscillations, Modes of Oscillations, Mode Curve (Qualitative Analysis only). **(Text 1: 9.1, 9.2.1)** **Microwave Transmission Lines:** Microwave Frequencies, Microwave devices, Microwave Systems, Transmission Line equations and solutions, Reflection Coefficient and Transmission Coefficient, Standing Wave and Standing Wave Ratio, Smith Chart, Single Stub matching. **(Text 2: 0.1, 0.2, 0.3, 3.1, 3.2, 3.3, 3.5, 3.6 Except Double stub matching**)	**L1,L2**
Module 2	
Microwave Network theory: Introduction**,** Symmetrical Z and Y-Parameters for reciprocal Networks, S matrix representation of Multi-Port Networks. **(Text1: 6.1, 6.2, 6.3)** **Microwave Passive Devices:** Coaxial Connectors and Adapters, Attenuators, Phase Shifters, Waveguide Tees, Magic tees. **(Text 1: 6.4.2, 6.4.14, 6.4.15, 6.4.16)**	**L1,L2**
Module 3	
Strip Lines: Introduction, Micro Strip lines, Parallel Strip lines, Coplanar Strip lines, Shielded Strip Lines**. (Text 2: 11.1, 11.2, 11.3, 11.4)** **Antenna Basics**: Introduction, Basic Antenna Parameters, Patterns, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Antenna Apertures, Effective Height, Radio Communication Link, Antenna Field Zones. **(Text 3: 2.1 - 2.7, 2.9 – 2.11, 2.13)**	**L1,L2,L3**
Module 4	
Point Sources and Arrays: Introduction, Point Sources, Power Patterns, Power Theorem, Radiation Intensity, Arrays of two isotropic point sources, Linear Arrays of n Isotropic Point Sources of equal Amplitude and Spacing.**(Text 3: 5.1 – 5.6, 5.9, 5.13)** **Electric Dipoles:** Introduction, Short Electric Dipole, Fields of a Short Dipole, Radiation Resistance of a Short Electric Dipole, Thin Linear Antenna (Field Analyses) **(Text 3: 6.1 - 6.5)**	**L1,L2,L3, L4**
Module 5	
Loop and Horn Antenna: Introduction, Small loop, The Loop Antenna General Case, The Loop Antenna as a special case, Radiation resistance of loops, Directivity of Circular Loop Antennas with uniform current, Horn antennas Rectangular Horn Antennas.**(Text 3: 7.1, 7.2, 7.4, 7.6, 7.7, 7.8, 7.19, 7.20)** **Antenna Types**: The Helix geometry, Helix modes, Practical Design considerations for the mono-filar axial mode Helical Antenna, Yagi-Uda array, Parabolic reflector **(Text 3: 8.3, 8.4, 8.5, 8.8, 9.5)**	**L1,L2,L3**

Course outcomes: At the end of the course students will be able to:

- Describe the use and advantages of microwave transmission
- Analyze various parameters related to microwave transmission lines and waveguides
- Identify microwave devices for several applications
- Analyze various antenna parameters necessary for building a RF system
- Recommend various antenna configurations according to the applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Microwave Engineering** – Annapurna Das, Sisir K Das, TMH, Publication, 2nd, 2010.
2. **Microwave Devices and circuits**- Samuel Y Liao, Pearson Education
3. **Antennas and Wave Propagation**- John D. Krauss, Ronald J Marhefka, Ahmad S Khan, 4th Edition, McGraw Hill Education, 2013

Reference Books:

1. **Microwave Engineering** - David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008.
2. **Microwave Engineering** – Sushrut Das, Oxford Higher Education, 2ndEdn, 2015
3. **Antennas and Wave Propagation** – Harish and Sachidananda: Oxford University Press, 2007

OPERATING SYSTEM

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC641**	**CIE Marks**	**40**
Number of LectureHours/Week	**03**	**SEE Marks**	**60**
Total Number ofLecture Hours	**40 (8 Hours /Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management.
- Describe the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

Module-1	**RBT Level**

Introduction to Operating Systems OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems**(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).**	**L1,L2**
Module-2	
Process Management: OS View of Processes, PCB, Fundamental State Transitions of a process, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux **(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text).**	**L1,L2,L3**
Module – 3	
Memory Management: Contiguous Memory allocation, Non-Contiguos Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux**(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text).**	**L1,L2,L3**
Module-4	
File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access **(Topics from Sections 7.1 to 7.8 of Text).**	**L1,L2**
Module-5	
Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention **(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).**	**L1,L2**

Course Outcomes: At the end of the course, the students will be able to:

- Explain the goals, structure, operation and types of operating systems.
- Apply scheduling techniques to find performance factors.
- Explain organization of file systems and IOCS.
- Apply suitable techniques for contiguous and non-contiguous memory allocation.
- Describe message passing, deadlock detection and prevention methods.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Operating Systems – A concept based approach, by Dhamdhere, TMH, 2nd edition.

Reference Books:

1. Operating systems concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2. Operating system–internals and design system, William Stalling, Pearson Education, 4th ed, 2006.
3. Design of operating systems, Tannanbhaum, TMH, 2001.

ARITIFICAL NEURAL NETWORKS
SEMESTER – VI (EC/TC)
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC642**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Human brain.
- Acquireknowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module-1	**RBT Level**
Introduction: Biological Neuron – Artificial Neural Model - Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. **Learning:** Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.	**L1, L2**
Module-2	
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Back propagation Learning Algorithm, Practical consideration of BP algorithm.	**L1,L2, L3**
Module-3	
Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.	**L1,L2, L3**
Module-4	

Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.	**L1,L2, L3**
Module-5	
Self-organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self-organization Feature Maps, Application of SOM, Growing Neural Gas.	**L1,L2, L3**

Course outcomes: At the end of the course, students should be able to:

- Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
- Understand the concepts and techniques of neural networks through the study of the most important neural network models.
- Evaluate whether neural networks are appropriate to a particular application.
- Apply neural networks to particular application, and to know what steps to take to improve performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Neural Networks A Classroom Approach– Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems**-J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks**-B. Yegnanarayana, PHI, New Delhi 1998.

OBJECT ORIENTED PROGRAMMING USING C++

SEMESTER – VI (EC/TC)

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC643**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: The objectives of this course are:

- Define Encapsulation, Inheritance and Polymorphism.
- Solve the problem with object oriented approach.
- Analyze the problem statement and build object oriented system model.
- Describe the characters and behavior of the objects that comprise a system.
- Explain function overloading, operator overloading and virtual functions.
- Discuss the advantages of object oriented programming over procedure oriented programming.

Module-1	**RBT Level**
Beginning with C++ and its features: What is C++?, Applications and structure of C++ program, Different Data types, Variables, Different Operators, expressions, operator overloading and control structures in C++ **(Topics from Ch-2,3 of Text).**	**L1, L2**
Module-2	
Functions, classes and Objects: Functions, Inline function, function overloading, friend and virtual functions, Specifying a class, C++ program with a class, arrays within a class, memory allocation to objects, array of objects, members, pointers to members and member functions **(Selected Topics from Chap-4,5 of Text).**	**L1,L2, L3**
Module-3	
Constructors, Destructors and Operator overloading: Constructors, Multipleconstructors in a class, Copy constructor, Dynamic constructor, Destructors, Defining operator overloading, Overloading Unary and binary operators, Manipulation of strings using operators **(Selected topics from Chap-6, 7 of Text)**.	**L1, L2, L3**
Module-4	
Inheritance, Pointers, Virtual Functions, Polymorphism: Derived Classes, Single, multilevel, multiple inheritance, Pointers to objects and derived classes, this pointer, Virtual and pure virtual functions **(Selected topics from Chap-8,9 of Text)**.	**L1, L2, L3**
Module-5	

Streams and Working with files: C++ streams and stream classes, formatted andunformatted I/O operations, Output with manipulators, Classes for file stream operations, opening and closing a file, EOF **(Selected topics from Chap-10, 11 of Text).**	**L1, L2, L3**

Course outcomes: At the end of the course, students should be able to:

- Explain the basics of Object Oriented Programming concepts.
- Apply the object initialization and destroy concept using constructors and destructors.
- Apply the concept of polymorphism to implement compile time polymorphism in programs by using overloading methods and operators.
- Use the concept of inheritance to reduce the length of code and evaluate the usefulness.
- Apply the concept of run time polymorphism by using virtual functions, overriding functions and abstract class in programs.
- Use I/O operations and file streams in programs.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Object Oriented Programming with C++, E.Balaguruswamy, TMH, 6th Edition, 2013.

Reference Books:

1. Object Oriented Programming using C++, Robert Lafore, Galgotia publication 2010.

DIGITAL SYSTEM DESIGN USING VERILOG

SEMESTER – VI EC

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC644**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**

Total Number of Lecture Hours	40 (08 Hrs per module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to

- Understand the concepts of Verilog Language.
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application.
- Design and diagnosis of processors and I/O controllers used in embedded systems.

Module -1	RBT Level
Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology **(1.1, 1.3 to 1.5 of Text).** **Combinational Basics:** Combinational Components and Circuits, Verification of Combinational Circuits **(2.3 and 2.4 of Text**). **Number Basics:** Unsigned integers, Signed Integers, Fixed point Numbers, Floating point Numbers **(3.1.1, 3.2.1, 3.3.1 and 3.4).** **Sequential Basics**: Sequential Datapaths and Control Clocked Synchronous Timing Methodology **(4.3 up to 4.3.1, 4.4 up to 4.4.1 of Text).**	**L1,L2, L3**
Module -2	
Memories: Concepts, Memory Types, Error Detection and Correction **(Chap 5 of Text).**	**L1,L2, L3**
Module -3	
Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity **(Chap 6 of Text).**	**L1,L2, L3**
Module -4	
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software **(Chap 8 of Text).**	**L1,L2, L3**
Module -5	
Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues **(Chap 10 of Text).**	**L1,L2, L3, L4**

Course outcomes: After studying this course, students will be able to:

- Construct the combinational circuits, using discrete gates and programmable logic devices.
- Describe how arithmetic operations can be performed for each kind of code, and also combinational circuits that implement arithmetic operations.
- Design a semiconductor memory for specific chip design.
- Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Synthesize different types of I/O controllers that are used in embedded system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

Reference Books:

1. Ming-Bo Lin, "Digital System Designs and Practices: Using Verilog HDL and FPGAs", Wiley, 2008
2. Charles Roth, Lizy K. John, "ByeongKilLeeDigital Systems Design Using Verilog, Cengage", Cengage, 1st Edition.
3. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer, Fifth edition.
4. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.

NANOELECTRONICS
SEMESTER – VI EC
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC645**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Enhance basic engineering science and technical knowledge of Nanoelectronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Know various nanostructures of carbon and the nature of the carbon bond itself.
- Learn the photo physical properties of sensor used in generating a signal.

Module-1	**RBT Level**
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moore's law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometerlength scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems**(Text 1).**	**L1, L2**
Module-2	
Characterization: Classification, Microscopic techniques, Field ion microscopy,scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques **(Text 1).** **Inorganic semiconductor nanostructures:** overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states **(Text 1).**	**L1, L2**
Module-3	
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations,	**L1, L2**

thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques.**(Text 1).** **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural **(Text 1).**	
Module-4	
Carbon Nanostructures: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes. **(Text 2)**	**L1, L2**
Module-5	
Nanosensors: Introduction, What is Sensor and Nanosensors?, What makes them Possible?, Order From Chaos, Characterization, Perception, NanosensorsBased On Quantum Size Effects, Electrochemical Sensors, Sensors Based On Physical Properties, Nanobiosensors, Smart dust Sensor for the future. **(Text 3)** **Applications:** Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS **(Text 1).**	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

- Understand the principles behind Nanoscience engineering and Nanoelectronics.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Know the properties of carbon and carbon nanotubes and its applications.
- Know the properties used for sensing and the use of smart dust sensors.
- Apply the knowledge to prepare and characterize nanomaterials.
- Analyse the process flow required to fabricate state-of-the-art transistor technology.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.
3. T Pradeep, "Nano: The essentials-Understanding Nanoscience and Nanotechnology", TMH.

Reference Book:

1. Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

EMBEDDED SYSTEMS LAB
SEMESTER – VI (EC/TC)
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18ECL66**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02 Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**
CREDITS – 02			

Course Learning Objectives: This course will enable students to:

- Understand the instruction set of ARM Cortex M3, a 32 bit microcontroller and the software tool required for programming in Assembly and C language.
- Program ARM Cortex M3 using the various instructions in assembly level language for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Laboratory Experiments

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn ALP and using evaluation version of Embedded 'C' &Keil uVision-4 tool/compiler.

PART A:

1. ALP to multiply two 16 bit binary numbers.
2. ALP to find the sum of first 10 integer numbers.
3. ALP to find the number of 0's and 1's in a 32 bit data
4. ALP to find determine whether the given 16 bit is even or odd
5. ALP to write data to RAM

PART B:

6. Display "Hello world" message using internal UART
7. Interface and Control the speed of a DC Motor.
8. Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
9. Interface a DAC and generate Triangular and Square waveforms.
10. Interface a 4x4 keyboard and display the key code on an LCD.
11. Demonstrate the use of an external interrupt to toggle an LED On/Off.
12. Display the Hex digits 0 to F on a 7-segment LED interface, with an appropriate delay.
13. Measure Ambient temperature using a sensor and SPI ADC IC.

Course outcomes: After studying this course, students will be able to:

- Understand the instruction set of 32 bit microcontroller ARM Cortex M3, and the software tool required for programming in Assembly and C language.
- Develop assembly language programs using ARM Cortex M3 for different applications.
- Interface external devices and I/O with ARM Cortex M3.
- Develop C language programs and library functions for embedded system applications.

Conduction of Practical Examination:

- One Question from PART A and one Question from PART B to be asked in the examination.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

COMMUNICATION LAB
SEMESTER – VI EC
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18ECL67**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Design and test the communication circuits for different analog modulation schemes.
- Design and demonstrate the digital modulation techniques
- Demonstrate and measure the wave propagation in microstrip antennas
- Characteristics of microstrip devices and measurement of its parameters.
- Understand the probability of error computations of coherent digital modulation schemes.

Laboratory Experiments

PART-A: Experiments No. 1 to 5 has to be performed using discrete components.

1. Amplitude Modulation and Demodulation: i) Standard AM, ii)DSBSC (LM741 and LF398 ICs can be used)
2. Frequency modulation and demodulation (IC 8038/2206 can be used)
3. Pulse sampling, flat top sampling and reconstruction
4. Time Division Multiplexing and Demultiplexing of two bandlimited signals.
5. FSK and PSK generation and detection
6. Measurement of frequency, guide wavelength, power, VSWR and attenuation in microwave test bench.
7. Obtain the Radiation Pattern and Measurement of directivity and gain of microstrip dipole and Yagi antennas.
8. Determination of
    a. Coupling and isolation characteristics of microstrip directional coupler.
    b. Resonance characteristics of microstrip ring resonator and computation of dielectric constant of the substrate.
    c. Power division and isolation of microstrip power divider.

PART-B: Simulation Experiments using SCILAB/MATLAB/Simulink or LabVIEW

1. Simulate NRZ, RZ, half-sinusoid and raised cosine pulses and generate eye diagram for binary polar signaling.
2. Pulse code modulation and demodulation system.
3. Computations of the Probability of bit error for coherent binary ASK, FSK and PSK for an AWGN Channel and Compare them with their Performance curves.
4. Digital Modulation Schemes i) DPSK Transmitter and receiver, ii) QPSK Transmitter and Receiver.

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Determine the characteristics and response of microwave waveguide.
- Determine the characteristics of microstrip antennas and devices and compute the parameters associated with it.

- Design and test the digital and analog modulation circuits and display the waveforms.
- Simulate the digital modulation systems and compare the error performance of basic digital modulation schemes.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from **PART-A** and one question from **PART-B or** only one question from **PART-B** experiments based on the complexity, to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

SIGNAL PROCESSING
SEMESTER – VI
[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC651**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**

CREDITS – 03

Course objective: This course will enable students to:

- Understand, represent and classify continuous time and discrete time signals and systems, together with the representation of LTI systems.
- Ability to represent continuous time signals (both periodic and non-periodic) in the time domain, s-domain and the frequency domain
- Understand the properties of analog filters, and have the ability to design Butterworth filters
- Understand and apply sampling theorem and convert a signal from continuous time to discrete time or from discrete time to continuous time (without loss of information)
- Able to represent the discrete time signal in the frequency domain
- Able to design FIR and IIR filters to meet given specifications

Module-1	**RBT Level**
Signal Definition, Signal Classification, System definition, System classification, for both continuous time and discrete time. Definition of LTI systems **(Chapter 1)**	**L1, L2**
Module-2	
Introduction to Fourier Transform, Fourier Series, Relating the Laplace Transform to Fourier Transform, Frequency response of continuous time systems, **(Chapter 3)**	**L1, L2**
Module-3	
Frequency response of ideal analog filters, Salient features of Butterworth filters Design and implementation of Analog Butterworth filters to meet given specifications **(Chapter 8)**	**L1,L2, L3**
Module-4	

Sampling Theorem- Statement and proof, converting the analog signal to a digital signal. Practical sampling. The Discrete Fourier Transform, Properties of DFT. Comparing the frequency response of analog and digital systems. (FFT not included) **(Chapter 3, 4)**	**L1,L2, L3**
Module-5	
Definition of FIR and IIR filters. Frequency response of ideal digital filters Transforming the Analog Butterworth filter to the Digital IIR Filter using suitable mapping techniques, to meet given specifications. Design of FIR Filters using the Window technique, and the frequency sampling technique to meet given specificationsComparing the designed filter with the desired filter frequency response **(Chapter 8)**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Understand and explain continuous time and discrete time signals and systems, in time and frequency domain
- Apply the concepts of signals and systems to obtain the desired parameter/ representation
- Analyse the given system and classify the system/arrive at a suitable conclusion
- Design analog/digital filters to meet given specifications
- Design and implement the analog filter using components/ suitable simulation tools *(assignment component)*
- Design and implement the digital filter (FIR/IIR) using suitable simulation tools, and record the input and output of the filter for the given audio signal *(assignment component)*

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

‘Signals and Systems’, by Simon Haykin and Barry Van Veen, Wiley.

References:

1. 'Theory and Application of Digital Signal Processing', Rabiner and Gold
2. ‘Signals and Systems’, Schaum’s Outline series
3. ‘Digital Signal Processing’, Schaum’s Outline series

SENSORS and SIGNAL CONDITIONING

SEMESTER – VI Open Elective A

[As per Choice Based Credit System (CBCS) System (CBCS) Scheme]

Course Code	**18EC652**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE marks**	**60**
Total Number of Lecture Hours	**40 (08 Hrs/module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand various technologies associated in manufacturing of sensors
- Acquire knowledge about types of sensors used in modern digital systems
- Get acquainted about material properties required to make sensors

Module 1	**RBT Level**
Introduction to sensor bases measurement systems: General concepts and terminology, sensor classification, primary sensors, material for sensors, microsensor technology, magnetoresistors, light dependent resistors, resistive hygrometers,resistive gas sensors, liquid conductivity sensors **(Selected topics from ch.1 & 2 of Text)**	**L1, L2**
Module 2	
Reactance Variation and Electromagnetic Sensors: -Capacitive Sensors, Inductive Sensors, Electromagnetic Sensors. **Signal Conditioning for Reactance Variation Sensors**-Problems and Alternatives, ac Bridges Carrier Amplifiers, Coherent Detection, Specific Signal Conditioners for Capacitive Sensors, Resolver-to-Digital and Digital-to-Resolver Converters.	**L1, L2**
Module 3	
Self-generating Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors.	**L2,L3**
Module 4	
Digital and intelligent sensors-position encoders, resonant sensors, sensors based on quartz resonators, SAW sensors, Vibrating wire strain gages, vibrating cylinder sensors, Digital flow meters.	**L2,L3**
Module 5	
Sensors based on semiconductor junctions -Thermometers based on semiconductor junctions, magneto diodes and magneto transistors, photodiodes and phototransistors, sensors based on MOSFET transistors, charge- coupled sensors – types of CCD imaging sensors, ultrasonic-based sensors.	**L2,L3**

Course Outcomes: After studying this course, students will be able to:

- Appreciate various types of sensors and their construction
- Use sensors specific to the end use application
- Design systems integrated with sensors

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"Sensors and Signal Conditioning", Ramon PallásAreny, John G. Webster, 2nd edition, John Wiley and Sons, 2000

BE 2018 Scheme Seventh Semester EC Syllabus

COMPUTER NETWORKS

B.E., VII Semester, Electronics & Communication Engineering

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC71**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1	**RBT Level**
Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. **(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text).** **Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. **(2.1, 2.2, 2.3 of Text)**	**L1, L2**
Module-2	
Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. **(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)** **Media Access Control:** Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text).** **Wired and Wireless LANs:** Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control**. (13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text)**	**L1,L2, L3**
Module-3	
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label. **(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)** **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text)**. **Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. **(20.1, 20.2of Text)**	**L1,L2, L3**
Module-4	
Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)** **Transport-Layer Protocols in the Internet:** User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control	**L1,L2, L3**

Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control. **(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text)**	
Module-5	
Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. **(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text)**	**L1, L2**

Course Outcomes: At the end of the course, the students will be able to:

- Understand the concepts of networking thoroughly
- Identify the protocols and services of different layers.
- Distinguish the basic network configurations and standards associated with each network.
- Analyze a simple network and measurement of its parameters.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

Forouzan, "Data Communications and Networking" , 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.

REFERENCE BOOKS:

1. James J Kurose, Keith W Ross, Computer Networks, , Pearson Education.
2. Wayarles Tomasi, Introduction to Data Communication and Networking,Pearson Education.
3. Andrew Tanenbaum, "Computer networks", Prentice Hall.
4. William Stallings, "Data and computer communications", Prentice Hall,

VLSI DESIGN

SEMESTER – VII EC

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC72**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1	**RBT Level**
Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)** **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics	**L1, L2**

(2.1, 2.2, 2.4 and 2.5 of TEXT2).	
Module-2	
Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).** MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1)**	**L1, L2,**
Module-3	
Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).** **Combinational Circuit Design:** Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**	**L1, L2, L3**
Module-4	
Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)** **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**	**L1, L2, L3**
Module-5	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), **(10.1 to 10.3 of TEXT1)** **Testing and Verification:** Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability **(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2).**	**L1, L2**

Course outcomes: At the end of the course, the students will be able to:

- Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
- Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
- Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
- Interpret Memory elements along with timing considerations
- Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.

2. "CMOS VLSI Design- A Circuits and Systems Perspective"- Neil H. E. Weste, and David Money Harris4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition,

Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Professional Elective – 2

REAL TIME SYSTEM
SEMESTER – VII (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC731**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**
Credits – 03			

Course Learning Objectives: This Course will enable students to:

- Understand the fundamentals of Real-time systems and its classifications.
- Describe the concepts of computer control and hardware components for Real-Time Application.
- Discuss the languages to develop software for Real-Time Applications.
- Explain the concepts of operating system and RTS development methodologies.

Module-1	**RBT Levels**
Introduction to Real-Time Systems: Historical background, Elements of a Computer Control System, RTS- Definition, Classification of Real-time Systems, Time Constraints, Classification of Programs. **Concepts of Computer Control:** Introduction, Sequence Control, Loop Control, Supervisory Control, Centralized Computer Control, Hierarchical Systems. **(Text: 1.1 to 1.6 and 2.1 to 2.6)**	**L1, L2**
Module-2	
Computer Hardware Requirements for Real-Time Applications: Introduction, General Purpose Computer, Single Chip Microcomputers and Microcontrollers, Specialized Processors, Process-Related Interfaces, Data Transfer Techniques, Communications, Standard Interface. **(Text: 3.1 to 3.8).**	**L1, L2**
Module-3	
Languages for Real-Time Applications: Introduction, Syntax Layout and Readability, Declaration and Initialization of Variables and Constants, Cutlass, Modularity and Variables, Compilation of Modular Programs, Data types, Control Structures, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device Handling, Concurrency, Real-Time Support, Overview of Real-Time Languages. **(Text: 5.1 to 5.14).**	**L1,L2, L3**
Module-4	
Operating Systems: Introduction, Real-Time Multi-Tasking OS, Scheduling Strategies, Priority Structures, Task Management, Scheduler and Real-Time Clock Interrupt Handler, Memory Management, Code Sharing, Resource Control, Task Co-Operation and Communication, Mutual Exclusion.**(Text: 6.1 to 6.11).**	**L1, L2**
Module-5	
Design of RTS – General Introduction: Introduction, Specification Document, Preliminary	**L1, L2, L3**

Design, Single-Program Approach, Foreground/Background System.
RTS Development Methodologies: Introduction, Yourdon Methodology, Ward and Mellor Method, Hately and Pirbhai Method.
(Text: 7.1 to 7.5 and 8.1, 8.2, 8.4,8.5).

Course Outcomes: At the end of the course, students should be able to:

- Explain the fundamentals of Real time systems and its classifications.
- Understand the concepts of computer controland the suitable computer hardware requirements for real-time applications.
- Describe the operating system concepts and techniques required for real time systems.
- Develop the software algorithmsusing suitable languages to meet Real time applications.
- Apply suitable methodologies to design and develop Real-Time Systems.

Text Book:

Real-Time Computer Control, by Stuart Bennet, 2nd Edn. Pearson Education. 2008.

Reference Books:

1. C.M. Krishna, Kang G. Shin, "Real –Time Systems", McGraw –Hill International Editions, 1997.
2. Real-Time Systems Design and Analysis, Phillip. A. Laplante, second edition, PHI, 2005.
3. Embedded Systems, Raj Kamal, Tata McGraw Hill, India, third edition, 2005.

SATELLITE COMMUNICATION
SEMESTER – VII (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC732**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to

- Understand the basic principle of satellite orbits and trajectories.
- Study of electronic systems associated with a satellite and the earth station.
- Understand the various technologies associated with the satellite communication.
- Focus on a communication satellite and the national satellite system.
- Study of satellite applications focusing various domains services such as remote sensing, weather forecasting and navigation.

Module-1	RBT Level
Satellite Orbits and Trajectories: Definition, Basic Principles, Orbital parameters, Injection velocity and satellite trajectory, Types of Satellite orbits, Orbital perturbations, Satellite stabilization, Orbital effects on satellite's performance, Eclipses, Look angles: Azimuth angle, Elevation angle.	**L1, L2**
Module-2	
Satellite subsystem: Power supply subsystem, Attitude and Orbit control, Tracking, Telemetry and command subsystem, Payload. **Earth Station:** Types of earth station, Architecture, Design considerations, Testing, Earth station Hardware, Satellite tracking.	**L1, L2**
Module-3	
Multiple Access Techniques: Introduction, FDMA (No derivation), SCPC Systems, MCPC Systems, TDMA, CDMA, SDMA. **Satellite Link Design Fundamentals**: Transmission Equation, Satellite Link Parameters, Propagation considerations	**L1,L2, L3**
Module-4	
Communication Satellites: Introduction, Related Applications, Frequency Bands, Payloads, Satellite Vs. Terrestrial Networks, Satellite Telephony, Satellite Television, Satellite radio, Regional satellite Systems, National Satellite Systems.	**L1, L2**
Module-5	
Remote Sensing Satellites: Classification of remote sensing systems, orbits, Payloads, Types of images: Image Classification, Interpretation, Applications. **Weather Forecasting Satellites**: Fundamentals, Images, Orbits, Payloads, Applications. **Navigation Satellites**: Development of Satellite Navigation Systems, GPS system, Applications.	**L1,L2, L3**

Course Outcomes: At the end of the course, the students will be able to:

- Describe the satellite orbits and its trajectories with the definitions of parameters associated with it.
- Describe the electronic hardware systems associated with the satellite subsystem and earth station.
- Describe the various applications of satellite with the focus on national satellite system.
- Compute the satellite link parameters under various propagation conditions with the illustration of multiple access techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Anil K. Maini, Varsha Agrawal, Satellite Communications, Wiley India Pvt. Ltd., 2015, ISBN: 978-81-265-2071-8.

Reference Books :

1. Dennis Roddy, Satellite Communications, 4th Edition, McGraw- Hill International edition, 2006
2. Timothy Pratt, Charles Bostian, Jeremy Allnutt, Satellite Communications, 2nd Edition, Wiley India Pvt. Ltd , 2017, ISBN: 978-81-265-0833-4

DIGITAL IMAGEPROCESSING

SEMESTER–VII(EC/TC)

[AsperChoiceBasedCreditSystem(CBCS)scheme]

CourseCode	18EC733	CIEMarks	40
Number ofLecture Hours/Week	03	SEEMarks	60
TotalNumberofLecture Hours	40 (08 Hours perModule)	ExamHours	03
CREDITS– 03			

CourseObjectives: This course will enable students to

- Understand the fundamentals of digital image processing.
- Understand the image transforms used in digital image processing.
- Understand the image enhancement techniques used in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.
- Understand the Morphological Operations used in digital image processing.

Module1	RBTLevel
DigitalImageFundamentals:WhatisDigitalImageProcessing?,OriginsofDigitalImageProcessing,Examplesoffieldsthatuse DIP,Fundamental StepsinDigitalImageProcessing,ComponentsofanImageProcessing System,ElementsofVisualPerception,ImageSensingandAcquisition **(Text:Chapter1andChapter2:Sections2.1to2.2,2.6.2)**	L1,L2
Module-2	

Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters **(Text: Chapter 2: Sections 2.3 to 2.62, Chapter 3: Sections 3.2 to 3.6)**	**L1, L2**
Module-3	
Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-D DFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering. **(Text: Chapter 4: Sections 4.2, 4.5 to 4.10)**	**L1, L2**
Module-4	
Restoration: Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position-Invariant degradations, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least Squares Filtering. **(Text: Chapter 5: Sections 5.2, to 5.9)**	**L1, L2**
Module-5	
Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing. Color Image Processing: Color Fundamentals, Color Models, Pseudocolor Image Processing. **(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections 9.1 to 9.3)**	**L1, L2**

Course Outcomes: At the end of the course, students should be able to:

- Understand image formation and the role human visual system plays in perception of gray and color image data.
- Apply image processing techniques in both the spatial and frequency (Fourier) domains.
- Design and evaluate image analysis techniques
- Conduct independent study and analysis of Image Enhancement and restoration techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

DigitalImageProcessing-RafelCGonzalezandRichardE.Woods,PHI3rd Edition 2010.

ReferenceBooks:

1. DigitalImageProcessing-S.Jayaraman,S.Esakkirajan,T.Veerakumar,TataMcGrawHill2014.
2. FundamentalsofDigitalImageProcessing-A.K.Jain,Pearson2004.
3. Image Processing analysis and Machine vision with MindTap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

DATA STRUCTURES USING C++

B.E., VII Semester (EC/TC)

[Choice Based Credit System (CBCS) scheme]

Course Code	**18EC734**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to

- Explain fundamentals of data structures and their applications essential for programming/problem solving
- Analyze Linear Data Structures: Stack, Queues, Lists
- Analyze Non Linear Data Structures: Trees
- Assess appropriate data structure during program development/Problem Solving

Module -1	**RBT Level**
INTRODUCTION: Functions and parameters, Dynamic memory allocation, Recursion. **LINEAR LISTS:** Data objects and structures, Linear list data structures, Array Representation, Vector Representation, Singly Linked lists and chains.	**L1, L2**
Module -2	

ARRAYS AND MATRICS: Arrays, Matrices, Special matrices, Sparse matrices. **STACKS:** The abstract data types, Array Representation, Linked Representation, and Applications- Parenthesis Matching & Towers of Hanoi.	**L1, L2**
Module -3	
QUEUES: The abstract data types, Array Representation, Linked Representation, Applications- Railroad car arrangement. **HASHING:** Dictionaries, Linear representation, Hash table representation.	**L1, L2, L3**
Module -4	
BINARY AND OTHER TREES: Trees, Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT binary tree and the class linked binary tree.	**L1,L2, L3**
Module -5	
Priority Queues: Linear lists, Heaps, Applications-Heap Sorting. **Search Trees:** Binary search trees operations and implementation, Binary Search trees with duplicates.	**L1, L2,L3**

Course outcomes: After studying this course, students will be able to:

- Acquire knowledge of Dynamic memory allocation, Various types of data structures, operations and algorithms and Sparse matrices and Hashing
- Understand non Linear data structures trees and their applications
- Design appropriate data structures for solving computing problems
- Analyze the operations of Linear Data structures: Stack, Queue and Linked List and their applications

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Eachfull questioncanhave a maximum of 4sub questions.
- There will be2 full questionsfromeachmodule coveringall the topics ofthe module.
- Students will havetoanswer 5full questions,selecting onefullquestionfrom each module.
- The total markswill beproportionally reduced to 60marksasSEEmarksis 60.

Text Book:

Data structures, Algorithms, and applications in C++, Sartaj Sahni, Universities Press, 2nd Edition, 2005.

Reference Books:

1. **Data structures, Algorithms, and applications in C++,** Sartaj Sahni, Mc. Graw Hill, 2000.
2. **Object Oriented Programming with C++,** E.Balaguruswamy**,** TMH, 6th Edition, 2013.
3. **Programming in C++,** E.Balaguruswamy. TMH, 4th, 2010.

DSP ALGORITHMS and ARCHITECTURE
VII Semester (EC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC735**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Figure out the knowledge and concepts of digital signal processing techniques.
- Understand the computational building blocks of DSP processors and its speed issues.
- Understand the various addressing modes, peripherals, interrupts and pipelining structure of TMS320C54xx processor.
- Learn how to interface the external devices to TMS320C54xx processor in various modes.
- Understand basic DSP algorithms with their implementation.

Module -1	**RBT Level**
Introduction to Digital Signal Processing: Introduction, A Digital Signal – Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Computational Accuracy in DSP Implementations:** Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.	**L1,L2**
Module -2	
Architectures for Programmable Digital Signal – Processing Devices: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.	**L1,L2**
Module -3	
Programmable Digital Signal Processors: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On – Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.	**L1,L2**
Module -4	

Implementation of Basic DSP Algorithms: Introduction, The Q – notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit – Reversed Index. Generation & Implementation on the TMS32OC54xx.	**L1,L2**
Module -5	
Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). **Interfacing and Applications of DSP Processors:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System.	**L1,L2**

Course Outcomes: At the end of this course, students would be able to

- Comprehend the knowledge and concepts of digital signal processing techniques.
- Apply the knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.
- Apply knowledge of various types of addressing modes, interrupts, peripherals and pipelining structure of TMS320C54xx processor.
- Develop basic DSP algorithms using DSP processors.
- Discuss about synchronous serial interface and multichannel buffered serial port (McBSP) of DSP device.
- Demonstrate the programming of CODEC interfacing.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

Reference Books:

1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002.
2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010
3. "Architectures for Digital Signal Processing", Peter Pirsch John Wiley, 2008

Professional Electives – 3

IoT & WIRELESS SENSOR NETWORKS
B.E., VII Semester(EC/TC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18EC741	CIE Marks	40
Number of Lecture Hours/Week	03	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IOT / WSNs.

Module-1	RBT Levels
Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.	**L1, L2**
Module-2	
Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports. **Data Collection, Storage and Computing using a Cloud Platform:** Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.	**L1, L2**
Module-3	
Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development. Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1.	**L1, L2, L3**
Module-4	

Overview of Wireless Sensor Networks: Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks. **Architectures**: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.	**L1, L2, L3**
Module-5	
Communication Protocols: Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.	**L1, L2, L3**

Course Outcomes: At the end of the course, students will be able to:

- Understand choice and application of IoT & M2M communication protocols.
- Describe Cloud computing and design principles of IoT.
- Awareness of MQTT clients, MQTT server and its programming.
- Develop an architecture and its communication protocols of of WSNs.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Eachfull questioncanhave a maximum of 4sub questions.
- There will be2 full questionsfromeachmodule coveringall the topics ofthe module.
- Students will havetoanswer 5full questions,selecting onefullquestionfrom each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols, And Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

AUTOMOTIVE ELECTRONICS
B.E., VII Semester (EC/TC)

[Choice Based Credit System (CBCS) scheme]

Course Code	18EC742	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours/Module)	Exam Hours	03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the basics of automobile dynamics and design electronics to complement those features.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts.

Module -1	RBT Level
Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System - Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train - Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System (Text 1: Chapter1), Starter Battery –Operating principle: **(Text 2: Pg. 407-410)** **The Basics of Electronic Engine Control –** Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition. **(Text 1: Chapter 5)**	**L1, L2**
Module -2	
Automotive Sensors – Automotive Control System applications of Sensors and Actuators – Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O2/EGO) Lambda Sensors, Piezoelectric Knock Sensor. **(Text 1: Chapter 6)** **Automotive Engine Control Actuators –** Solenoid, Fuel Injector, EGR Actuator, Ignition System **(Text 1: Chapter 6)**	**L1, L2**
Module -3	
Digital Engine Control Systems – Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control - Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System - Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics. **(Text 1: Chapter 7)** **Control Units –** Operating conditions, Design, Data processing, Programming, Digital modules in the Control unit, Control unit software. **(Text 2: Pg. 196-207)**	**L1, L2**
Module -4	
Automotive Networking –Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles **(Text 2: Pg. 85-91),** Buses - CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. **(Text 2: Pg. 92-151)** **Vehicle Motion Control** – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS) **(Text 1: Chapter 8)**	**L1,L2**

Module -5	
Automotive Diagnostics–Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems, Occupant Protection Systems – Accelerometer based Air Bag systems. **(Text 1: Chapter 10)** **Future Automotive Electronic Systems** – Alternative Fuel Engines, Electric and Hybrid vehicles, Fuel cell powered cars, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Heads Up display, Speech Synthesis, Navigation – Navigation Sensors - Radio Navigation, Signpost navigation, dead reckoning navigation, Voice Recognition Cell Phone dialing, Advanced Cruise Control, Stability Augmentation, Automatic driving Control **(Text 1: Chapter 11)**	**L1, L2,L3**

Course Outcomes: At the end of the course, students will be able to:

- Acquire an overview of automotive components, subsystems, and basics of Electronic Engine Control in today's automotive industry.
- Use available automotive sensors and actuators while interfacing with microcontrollers / microprocessors during automotive system design.
- Understand the networking of various modules in automotive systems, communication protocols and diagnostics of the sub systems.
- Design and implement the electronics that attribute the reliability, safety, and smartness to the automobiles, providing add-on comforts and get fair idea on future Automotive Electronic Systems.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Eachfull questioncanhave a maximum of 4sub questions.
- There will be2 full questionsfromeachmodule coveringall the topics ofthe module.
- Students will havetoanswer 5full questions,selecting onefullquestionfrom each module.
- The total markswill beproportionally reduced to 60marksasSEEmarksis 60.

Text Books:

1. William B. Ribbens, "Understanding Automotive Electronics", 6th Edition, Elsevier Publishing.
2. Robert Bosch Gmbh (Ed.) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley& Sons Inc., 2007.

MULTIMEDIA COMMUNICATION
VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC743	CIE Marks	40
Number of Lecture Hours/Week	03	Exam Marks	60
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the importance of multimedia in today's online and offline information sources and repositories.
- Understand the how Text, Audio, Image and Video information can be represented digitally in a computer so that it can be processed, transmitted and stored efficiently.
- Understand the Multimedia Transport in Wireless Networks
- Understand the Real-time multimedia network applications.
- Understand the Different network layer based application.

Module -1	RBT Level
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology. (**Chapter 1 of Text 1)**	**L1,L2**
Module -2	
Information Representation: Introduction, Digitizationprinciples, Text, Images,AudioandVideo.**(Chapter 2 of Text 1)**	**L1,L2**
Module -3	
Text and Image Compression: Introduction,Compressionprinciples,textcompression,imageCompression.**(Chapter 3 of Text 1)** **Distributed Multimedia Systems:**Introduction,mainFeaturesofaDMS, Resourcemanagementof DMS,Networking,Multimedia Operating Systems. **(Chapter 4 - Sections 4.1 to 4.5 of Text 2)**	**L1,L2**
Module -4	
Audio and video compression: Introduction, Audiocompression, video compression,videocompressionprinciples,videocompression.**(Chapter 4 of Text 1)**	**L1,L2**
Module -5	
Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring,Bridges, FDDIHigh-speed LANs,LANprotocol**(Chap. 8 of Text 1).** **The Internet:**Introduction,IPDatagrams,Fragmentation,IPAddress,ARP and RARP, QoS Support, IPv8.**(Chap. 9 of Text 1)**	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks and applications.
- Understand different compression techniques to compress audio and video.
- Describe multimedia Communication across Networks.
- Analyse different media types to represent them in digital form.
- Compress different types of text and images using different compression techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Multimedia Communications- Fred Halsall, Pearson Education, 2001, ISBN -9788131709948.
2. Multimedia Communication Systems- K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, Pearson Education, 2004. ISBN -9788120321458.

Reference Book:

Multimedia:Computing,Communicationsand Applications- Raifsteinmetz,KlaraNahrstedt,Pearson Education,2002.ISBN-978817758

CRYPTOGRAPHY
VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC744**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Explain classical cryptography algorithms.
- Acquire knowledge of mathematical conceptsrequired for cryptography.
- Describe pseudo random sequence generation technique.
- Explain symmetric and asymmetric cryptography algorithms.

Module -1	**RBT Level**
Classical Encryption Techniques: Symmetric cipher model, Substitutiontechniques, Transposition techniques **(Text 1: Chapter 1)** **Basic Concepts of Number Theory and Finite Fields:** Euclidean algorithm,Modular arithmetic **(Text 1: Chapter 3)**	**L1,L2**
Module -2	
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryptionstandard (DES), The AES Cipher. **(Text 1: Chapter 2: Section1, 2, Chapter 4:Section 2, 3, 4)**	**L1,L2**
Module -3	
Basic Concepts of Number Theory and Finite Fields: Groups, Rings andFields, Finite fields of the form GF(p), Prime Numbers, Fermat's and Euler'stheorem, discrete logarithm. **(Text 1: Chapter 3 and Chapter 7: Section 1, 2, 5)**	**L1,L2**
Module -4	
ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSAalgorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, EllipticCurve Cryptography **(Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)**	**L1,L2,L3**
Module -5	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design andanalysis of stream ciphers, Stream ciphers using LFSRs, A5, HughesXPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M,PKZIP **(Text 2: Chapter 16**)	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain basic cryptographic algorithms to encrypt and decrypt the data.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the information.
- Apply concepts of modern algebra in cryptography algorithms.
- Apply pseudo random sequence in stream cipher algorithms.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles andPractice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, andSource code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

MACHINE LEARNING
VII Semester (EC/TC)

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC745**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Acquire some concepts and techniques that are core to Machine Learning.
- Understand learning and decision trees.
- Acquire knowledge of neural networks, Bayesian techniques and instant based learning.
- Understand analytical learning and reinforced learning.

Module -1	RBT Level
Learning: Designing Learning systems, Perspectives and Issues, Concept Learning, Version Spaces and Candidate Elimination Algorithm, Inductive bias.	**L1,L2**
Module -2	
Decision Tree and ANN: Decision Tree Representation, Hypothesis Space Search, Inductive bias in decision tree, issues in Decision tree. Neural Network Representation, Perceptrons, Multilayer Networks and Back Propagation Algorithms.	**L1,L2**
Module -3	
Bayesian and Computational Learning: Bayes Theorem, Bayes Theorem Concept Learning, Maximum Likelihood, Minimum Description Length Principle, Bayes Optimal Classifier, Gibbs Algorithm, Naïve Bayes Classifier.	**L1,L2**
Module -4	
Instant Based Learning and Learning set of rules: K- Nearest Neighbour Learning, Locally Weighted Regression, Radial Basis Functions, Case-Based Reasoning. Sequential Covering Algorithms, Learning Rule Sets, Learning First Order Rules, Learning Sets of First Order Rules.	**L1,L2**
Module -5	
Analytical Learning and Reinforced Learning: Perfect Domain Theories, Explanation Based Learning, Inductive-Analytical Approaches, FOCL Algorithm, Reinforcement Learning.	**L1,L2**

Course outcomes: At the end of the course, students should be able to:

- Understand the core concepts of Machine learning.
- Appreciate the underlying mathematical relationships within and across Machine Learning algorithms.
- Explain paradigms of supervised and un-supervised learning.
- Recognize a real world problem and apply the learned techniques of Machine Learning to solve the problem.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Machine Learning-Tom M. Mitchell, McGraw-Hill Education, (Indian Edition), 2013.

Reference Books:

1. **Introduction to Machine Learning-** Ethem Alpaydin, 2nd Ed., PHI Learning Pvt. Ltd., 2013.
2. **The Elements of Statistical Learning-**T. Hastie, R. Tibshirani, J. H. Friedman, Springer; 1st edition, 2001.

COMPUTER NETWORKS LAB

SEMESTER – VII (EC)
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18ECL76**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**
CREDITS – 02			

Course Learning Objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.

i) Bit stuffing

ii) Character stuffing.

2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Use the network simulator for learning and practice of networking algorithms.
- Illustrate the operations of network protocols and algorithms using C programming.
- Simulate the network with different configurations to measure the performance parameters.
- Implement the data link and routing protocols using C programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination one question from software and one question from hardware or only one hardware experiments based on the complexity to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

VLSI LAB

B.E., VII Semester EC

[As per Choice Based Credit System (CBCS) Scheme]

Course Code	**18ECL77**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1. a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:
   a. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?
   b. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?
   c. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b)Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2.b)Draw layout of NAND withWp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3.a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

3. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4. a)Capture schematic of two-stage operational amplifier and measure the following:
   a. UGB
   b. dB bandwidth
   c. Gain margin and phase margin with and without coupling capacitance
   d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
   e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.

4. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1.Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:

a. Verify the functionality using test bench

b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2.Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.

3.Write verilog code for UART and carry out the following:

a. Perform functional verification using test bench

b. Synthesize the design targeting suitable library and by setting area and timing constraints

c. For various constrains set, tabulate the area, power and delay for the synthesized netlist

d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

4.Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.

a. Perform functional verification using test bench

b. Synthesize the design targeting suitable library by setting area and timing constraints

c. For various constrains set, tabulate the area, power and delay for the synthesized netlist

d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

Compare the synthesis results of ALU modeled using IF and CASE statements.

5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).

6.For the synthesized netlist carry out the following for any two above experiments:

a. Floor planning (automatic), identify the placement of pads

b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells

c. Physical verification and record the LVS and DRC reports

d. Perform Back annotation and verify the functionality of the design

e. Generate GDSII and record the number of masks and its color composition

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Design and simulate combinational and sequential digital circuits using Verilog HDL
- Understand the Synthesis process of digital circuits using EDA tool.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
- Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
- Perform RTL-GDSII flow and understand the stages in ASIC design.

OPEN ELECTIVE-B OFFERED BY EC/TC BOARD

COMMUNICATION THEORY

SEMESTER – Open Elective-B

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC751	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours/Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Describe essential elements of an electronic communications.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Explain thebasics of sampling and quantization.
- Understand the various digital modulation schemes.
- The concepts of wireless communication.

Module -1	RBT Level
Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation **(Text 1: 1.1 to1.10)**	**L1, L2**
Module -2	
Noise: Classification and source of noise **(TEXT1:3.1)** **Amplitude Modulation Techniques:**Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, **(TEXT 1: 4.1,4.2, 4.4, 4.6)** **Angle Modulation Techniques:** Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation **(TEXT1: 5.1,5.2, 5.5)** **Analog Transmission and Reception:** AM Radio transmitters, AM Radio Receivers **(TEXT1:6.1,6.2)**	**L1, L2**
Module -3	
Sampling Theorem and pulse Modulation Techniques: Digital Versus analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals **(TEXT 1: 7.1 to 7.8)**	**L1, L2**
Module -4	
Digital Modulation Techniques: Types of digital Modulation, ASK,FSK,PSK,QPSK **(TEXT 1: 9.1 to 9.5)** **Source and Channel Coding:**Objective of source coding, source coding technique, Shannon's source coding theorem, need of channel coding, Channel coding theorem, error control and coding **(TEXT 1: 11.1 to 11.3, 11.8, 11.9,11.12)**	**L1,L2**
Module -5	

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next-generation networks, Applications of wireless communication**(TEXT 2: 1.1 to 1.7)** **Principles of Cellular Communications:** Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequecy reuse distance**(TEXT 2: 4.1 to 4.7)**	**L1, L2**

Course Outcomes: At the end of the course, students will be able:

- Describe operation of communication systems.
- Understand the techniques of Amplitude and Angle modulation.
- Understand theconcept of sampling and quantization.
- Understand the concepts of different digital modulation techniques.
- Describe the principles of wireless communications system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Analog and Digital Communications by T L Singal, McGraw Hill Education (India) Private Limited.
2. Wireless Communications by T L Singal, McGraw Hill Education (India) Private Limited.

Reference Books:

1. Modern Digital and Analog Communication Systems B. P. Lathi, Oxford University Press., 4th ed, 2010,
2. Communication Systems: Analog and Digital, R.P.Singh and S.Sapre: TMH 2nd edition, 2007
3. Introduction to Wireless Telecommunications systems and Networks by Gray J Mullett, Cengage learning.

NEURAL NETWORKS
VII Semester – Open Elective-B

[As per Choice Based Credit System (CBCS) scheme]

Course Code	**18EC752**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Understand the basics of ANN and comparison with Human brain.
- Acquire knowledge on Generalization and function approximation of various ANN architectures.
- Understand reinforcement learning using neural networks
- Acquire knowledge of unsupervised learning using neural networks.

Module -1	RBT Level
Introduction: Biological Neuron – Artificial Neural Model -Types of activation functions – **Architecture**: Feedforward and Feedback, Convex Sets, Convex Hull and Linear Separability, Non-Linear Separable Problem. XOR Problem, Multilayer Networks. **Learning:** Learning Algorithms, Error correction and Gradient Descent Rules, Learning objective of TLNs, Perceptron Learning Algorithm, Perceptron Convergence Theorem.	**L1,L2**
Module -2	
Supervised Learning: Perceptron learning and Non Separable sets, α-Least Mean Square Learning, MSE Error surface, Steepest Descent Search, μ-LMS approximate to gradient descent, Application of LMS to Noise Cancelling, Multi-layered Network Architecture, Backpropagation Learning Algorithm, Practical consideration of BP algorithm.	**L1,L2,L3**
Module -3	
Support Vector Machines and Radial Basis Function: Learning from Examples, Statistical Learning Theory, Support Vector Machines, SVM application to Image Classification, Radial Basis Function Regularization theory, Generalized RBF Networks, Learning in RBFNs, RBF application to face recognition.	
Module -4	
Attractor Neural Networks: Associative Learning Attractor Associative Memory, Linear Associative memory, Hopfield Network, application of Hopfield Network, Brain State in a Box neural Network, Simulated Annealing, Boltzmann Machine, Bidirectional Associative Memory.	**L1,L2,L3**
Module -5	
Self -organization Feature Map: Maximal Eigenvector Filtering, Extracting Principal Components, Generalized Learning Laws, Vector Quantization, Self -organization Feature Maps, Application of SOM, Growing Neural Gas.	**L1,L2,L3**

Course outcomes: At the end of the course, students should be able to:

- Understand the role of neural networks in engineering, artificial intelligence, and cognitive modelling.
- Understand the concepts and techniques of neural networks through the study of the most important neural network models.
- Evaluate whether neural networks are appropriate to a particular application.
- Apply neural networks to particular application, and to know what steps to take to improve performance.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Neural Networks A Classroom Approach –Satish Kumar, McGraw Hill Education (India) Pvt. Ltd, Second Edition.

Reference Books:

1. **Introduction to Artificial Neural Systems -** J.M. Zurada, Jaico Publications 1994.
2. **Artificial Neural Networks-** B. Yegnanarayana, PHI, New Delhi 1998.

Wireless and Cellular Communication

VIII Semester EC

[As per Choice Based Credit System (CBCS) scheme]

Course Code	18EC81	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (08 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the concepts of propagation over wireless channels from a physics standpoint
- Application of Communication theory both Physical and networking to understand GSM systems that handle mobile telephony
- Application of Communication theory both Physical and networking to understand CDMA systems that handle mobile telephony.
- Application of Communication theory both Physical and networking to understand LTE-4G systems.

Module-1	RBT Level
Mobile Radio Propagation – Large Scale Path Loss - Free Space Propagation Model, Relating Power to Electric Field, Three Basic Propagation Mechanisms – Reflection (Ground Reflection) , Diffraction, Scattering, Practical Link Budget, **(Text 1 - 2.2 and Ref1 - Chapter 4).** **Fading and Multipath** – Broadband wireless channel, Delay Spread and Coherence Bandwidth, Doppler Spread and Coherence Time, Angular spread and Coherence Distance **(Text 1 – 2.4)** , Statistical Channel Model of a Broadband Fading Channel **(Text 1 – 2.5.1)** **The Cellular Concept** – Cellular Concept , Analysis of Cellular Systems, Sectoring **(Text 1-2.3)**	**L1, L2**
Module-2	
GSM and TDMA Technology **GSM System overview** – Introduction, GSM Network and System Architecture, GSM Channel Concept. **GSM System Operations** – GSM Identities, System Operations –Traffic cases, GSM Infrastructure Communications (Um Interface) **(Text 2, Part1 and Part 2 of Chapter 5)**	**L1,L2,L3**
Module-3	
CDMA Technology **CDMA System Overview** – Introduction, CDMA Network and System Architecture **CDMA Basics** – CDMA Channel Concepts, CDMA System (Layer 3) operations, 3G CDMA (**Text 2-Part 1, Part2 and Part 3 of Chapter 6)**	**L1,L2,L3**
Module-4	
LTE – 4G **Key Enablers for LTE 4G** – OFDM, SC-FDE, SC-FDMA, Channel Dependant Multiuser Resource Scheduling, Multi-Antenna Techniques, Flat IP Architecture, LTE Network Architecture. **(Text 1, Sec 1.4)** **Multi-Carrier Modulation –** Multicarrier concepts, OFDM Basics, OFDM in LTE, Timing and Frequency Synchronization, Peak to Average Ration, SC-Frequency Domain Equalization, Computational Complexity Advantage of OFDM and SC-FDE. **(Text 1, Sec 3.1 – 3.7)**	**L1,L2,L3**
Module-5	

LTE - 4G **OFDMA and SC-FDMA –** Multiple Access for OFDM Systems, OFDMA, SCFDMA, Multiuser Diversity and Opportunistic Scheduling, OFDMA and SC-FDMA in LTE, OFDMA system Design Considerations. **(Text 1, Sec 4.1 – 4.6)** **The LTE Standard –** Introduction to LTE and Hierarchical Channel Structure of LTE, Downlink OFDMA Radio Resources, Uplink SC-FDMA Radio Resources. **(Text 1, Sec 6.1 – 6.4)**	**L1, L2,L3**

Course Outcomes: After studying this course, students will be able to:

- Explain concepts of propagation mechanisms like Reflection, Diffraction, Scattering in wireless channels.
- Develop a scheme for idle mode, call set up, call progress handling and call tear down in a GSM cellular network.
- Develop a scheme for idle mode, call set up, call progress handling and call tear down in a CDMA cellular network.
- Understand the Basic operations of Air interface in a LTE 4G system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Fundamentals of LTE" ArunabhaGhosh, Jan Zhang, Jefferey Andrews, Riaz Mohammed, Pearson education (FormerlyPrentice Hall, Communications Engg and Emerging Technologies), ISBN-13: 978-0-13-703311-9.
2. "Introduction to Wireless Telecommunications Systems and Networks", Gary Mullet, First Edition, Cengage Learning India Pvt Ltd., 2006, ISBN - 13: 978-81-315-0559-5.

Reference Books:

1. "Wireless Communications: Principles and Practice" Theodore Rappaport, 2nd Edition, Prentice Hall Communications Engineering and Emerging Technologies Series, 2002, ISBN 0-13-042232-0.
2. LTE for UMTS Evolution to LTE-Advanced' HarriHolma and AnttiToskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003. 2

NETWORK SECURITY
VIII Semester EC/TC

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	**18EC821**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enablestudents to:

- Describe network security services and mechanisms.
- Understand Transport Level Security and Secure Socket Layer
- Know about Security concerns in Internet Protocol security
- Discuss about Intruders, Intrusion detection and Malicious Software
- Discuss about Firewalls, Firewall characteristics, Biasing and Configuration

Module-1	**RBT Level**

AttacksonComputersandComputerSecurity:Needfor Security,SecurityApproaches,PrinciplesofSecurityTypesofAttacks. **(Chapter1-Text2)**	**L1, L2**
Module-2	
TransportLevelSecurity:WebSecurityConsiderations, SecureSocketsLayer,TransportLayerSecurity,HTTPS,SecureShell (SSH)**(Chapter15-Text1)**	**L1,L2**
Module-3	
IP Security: Overview of IP Security (IPSec),IP Security Architecture, Modes of Operation, Security Associations (SA), Authentication Header (AH), Encapsulating Security Payload (ESP), InternetKey Exchange. **(Chapter19-Text1)**	**L1,L2**
Module-4	
Intruders, Intrusion Detection.**(Chapter20-Text1)** **MALICIOUS SOFTWARE:**Viruses and Related Threats, Virus Countermeasures, **(Chapter21-Text1)**	**L1,L2**
Module-5	
Firewalls: The Need for firewalls, Firewall Characteristics, Types of Firewalls, Firewall Biasing, Firewall location andconfiguration **(Chapter22-Text 1)**	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

- Explain network security services and mechanisms and explain security concepts
- Understand the concept of Transport Level Security and Secure Socket Layer.
- Explain Security concerns in Internet Protocol security
- Explain Intruders, Intrusion detection and Malicious Software
- Describe Firewalls, Firewall Characteristics, Biasing and Configuration

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1.CryptographyandNetworkSecurityPrinciplesandPractice‖,PearsonEducationInc., William Stallings, 5th Edition, 2014, ISBN: 978-81-317- 6166-3.
2.Cryptography and Network Security, AtulKahate, TMH, 2003.

REFERENCE BOOKS:

1.Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.

MICRO ELECTROMECHANICAL SYSTEMS

VIII Semester, EC/TC

[As per Choice Based Credit System (CBCS)Scheme]

Course Code	**18EC822**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Objectives: This course will enablestudents to:

- Understand overview of microsystems, their fabrication and application areas.
- Working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices.
- Know methods to fabricate MEMS devices.
- Various applicationareas where MEMS devices can be used.

Module-1	**RBT Level**
OverviewofMEMSandMicrosystems:MEMSandMicrosystem,Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems andMicroelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	**L1, L2**
Module-2	
Working Principles of Microsystems: Introduction, Microsensors,Microactuation, MEMS with Microactuators,Microaccelerometers, Microfluidics. **Engineering Science for Microsystems Design and Fabrication:**Introduction, Molecular Theory of Matter and Inter-molecular Forces, Plasma Physics, Electrochemistry.	**L1,L2**
Module-3	
Engineering Mechanicsfor Microsystems Design: Introduction, StaticBending ofThin Plates, Mechanical Vibration, Thermo mechanics, Fracture Mechanics, Thin Film Mechanics, Overview on FiniteElement Stress Analysis.	**L1,L2**
Module-4	
Scaling Laws in Miniaturization: Introduction, ScalinginGeometry, Scaling in Rigid-Body Dynamics, Scalingin Electrostatic Forces, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	**L1,L2**
Module-5	

OverviewofMicromanufacturing:Introduction,BulkMicromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micro manufacturing.	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

- Appreciate the technologies related to Micro Electro Mechanical Systems.
- Understand design and fabricationprocesses involved with MEMS Devices.
- Analyze the MEMS devices and develop suitable mathematical models Know various application areas for MEMS device

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Tai-Ran Hsu, MEMSand Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

Reference Books:

1. Hans H. Gatzen,Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cenage Learning.

RADAR ENGINEERING

VIII Semester,EC/TC

[As per Choice Based Credit System (CBCS)Scheme

Course Code	**18EC823**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objectives: This course will enable students to:

- Understand the Radar fundamentals and analyze the radar signals.
- Understandvarioustechnologiesinvolvedinthedesignofradartransmittersand receivers.
- Learn various radars like MTI, Doppler and tracking radars and their comparison

Module-1	RBT Level
BasicsofRadar: Introduction,MaximumUnambiguousRange,RadarWaveforms, Definitionswithrespecttopulsewaveform-PRF,PRI,DutyCycle,PeakTransmitter Power, Average transmitter Power.Simple form of the Radar Equation, Radar Block Diagram and Operation, RadarFrequencies, Applications of Radar, TheOrigins of Radar, Illustrative Problems. **(Chapter 1 of Text)**	**L1, L2,L3**
Module-2	
TheRadarEquation:PredictionofRange`Performance,DetectionofsignalinNoise, MinimumDetectableSignal,ReceiverNoise,SNR,ModifiedRadarRangeEquation, Envelope Detector —False Alarm Time and Probability, Probability of Detection,Radar Cross Section of Targets:simple targets –sphere, cone-sphere, Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), IllustrativeProblems. **(Chapter 2 of Text, Except 2.4, 2.6, 2.8 & 2.11)**	**L1,L2,L3**
Module-3	
MTI and Pulse Doppler Radar: Introduction, Principle, Doppler Frequency Shift,Simple CW Radar, Sweep to Sweep subtraction and Delay Line Canceler, MTIRadar with– PowerAmplifierTransmitter,DelayLineCancelers— FrequencyResponseof Single Delay- Line Canceler, Blind Speeds,ClutterAttenuation,MTI Improvement Factor, N- Pulse Delay-Line Canceler,Digital MTI Processing–Blind phases, I and Q Channels, Digital MTIDoppler signalprocessor, Moving Target Detector- Original MTD. **(Chapter 3: 3.1, 3.2, 3.5, 3.6 of Text)**	**L1,L2,L3**
Module-4	
Tracking Radar: Tracking with Radar- Types of Tracking Radar Systems, MonopulseTracking- Amplitude Comparison Monopulse(one-and two-coordinates), Phase Comparison Monopulse. Sequential Lobing, Conical Scan Tracking, Block Diagram of Conical Scan Tracking Radar, Tracking in Range, Comparison of Trackers.**(Chapter4: 4.1, 4.2, 4.3 of Text)**	**L1,L2,L3**
Module-5	
TheRadarAntenna: FunctionsofTheRadarAntenna,AntennaParameters,ReflectorAntennasandElectronicallySteeredPhasedarrayAntennas.(Chapter9:9.1,9.29.4, 9.5 of Text) **Radar Receiver:**The Radar Receiver, Receiver Noise Figure, Super HeterodyneReceiver, Duplexers and Receivers Protectors, Radar Displays. **(Chapter 11 of Text)**	**L1, L2,L3**

Course outcomes:At the end of the course, students will be able to:

- Understand the radar fundamentals and radar signals.
- Explaintheworkingprincipleofpulse Dopplerradars,theirapplicationsand limitations
- Describe the working of various radar transmitters andreceivers.
- Analyzetherangeparametersofpulseradarsystemwhichaffectthesystem performance

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOK:

Introduction to Radar Systems- Merrill I Skolink, 3e, TMH, 2001

REFERENCE BOOKS:

1. RadarPrinciples,Technology,Applications—ByronEdde,Pearson Education, 2004.
2. Radar Principles–Peebles. Jr, P.Z. Wiley. New York, 1998.
3. Principles of Modem Radar: Basic Principles–Mark A. Rkhards, James A. Scheer, William A. HoIm. Yesdee, 2013

OPTICAL COMMUNICATION NETWORKS

VIII Semester EC
[As per Choice Based Credit System (CBCS) Scheme]

Course Code	18EC824	CIE Marks	40
Number of LectureHours/Week	3	SEE Marks	60
Total Number ofLecture Hours	40 (8 Hours / Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Learn the basic principle of optical fiber communication with different modes of light propagation.
- Understand the transmission characteristics and losses in optical fiber.
- Study of optical components and its applications in optical communication networks.
- Learn the network standards in optical fiber and understand the network architectures along with its functionalities.

Module -1	RBT Level
OpticalfiberCommunications: Historical development, The general system, Advantages of opticalfiber communication, Opticalfiberwaveguides:Raytheorytransmission,Modesinplanar guide, Phase and group velocity,Cylindricalfiber:Modes, Step index fibers, Graded index fibers, Single mode fibers, Cutoff wavelength, Mode field diameter, effective refractive index. Fiber Materials, Photonic crystal fibers.**(Text 2)**	**L1, L2**
Module -2	

Transmissioncharacteristicsofopticalfiber: Attenuation, Materialabsorptionlosses,Linearscatteringlosses,Nonlinearscattering losses, Fiber bend loss, Dispersion, Chromatic dispersion, Intermodal dispersion: Multimode step index fiber. **OpticalFiberConnectors:**Fiberalignmentandjointloss,Fiber splices: Fusion Splices, Mechanical splices, Fiber connectors: Cylindrical ferrule connectors, Duplex and Multiple fiber connectors, Fibercouplers: three and four port couplers,star couplers, Optical Isolators and Circulators**.(Text 2)**	**L1, L2**
Module -3	
Optical sources: LightEmittingdiodes:LEDStructures,Light Source Materials, Quantum Efficiency and LED Power, Modulation. LaserDiodes:ModesandThresholdconditions, Rate equation, External Quantum Efficiency, ResonantFrequencies.	**L1, L2**
Photodetectors: Physical principles of Photodiodes, Photo detector noise, Detector response time. **Optical Receiver:** Optical Receiver Operation: Error sources, Front End Amplifiers, Receiver sensitivity, Quantum Limit.**(Text1)**	
Module -4	
WDM Concepts and Components: Overview of WDM: Operational Principles of WDM, WDM standards, Mach-Zehnder Interferometer Multiplexers, Isolators and Circulators, Fiber grating filters, Dielectric Thin-Film Filters, Diffraction Gratings. Optical amplifiers: Basic application and Types, Semiconductor optical amplifiers, Erbium Doped Fiber Amplifiers, Raman Amplifiers, Wideband Optical Amplifiers. **(Text 1)**	**L1, L2**
Module -5	
Optical Networks: Optical network evolution and concepts: Optical networking terminology, Optical network node and switching elements, Wavelength division multiplexed networks, Public telecommunication network overview. Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, OSI reference model, Optical transport network, Internet protocol, Wavelength routing networks: Routing and wavelength assignment, Optical switching networks: Optical circuit switched networks, packet switched networks, Multiprotocol Label Switching, Optical burst switching networks.**(Text 2)**	**L1, L2**

Course Outcomes: At the end of the course, students will be able to:

- Classification and working of optical fiber with different modes of signal propagation.
- Describe the transmission characteristics and losses in optical fiber communication.
- Describe the construction and working principle of optical connectors, multiplexers and amplifiers.
- Describe the constructional features and the characteristics of optical Sources and detectors.
- Illustrate the networking aspects of optical fiber and describe various standards associated with it.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each modulecovering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- Thetotalmarkswillbeproportionallyreducedto60marksasSEE marks is 60.

Text Books:

1.Gerd Keiser , Optical Fiber Communication, 5th Edition, McGraw Hill Education(India) Private Limited, 2015. ISBN:1-25-900687-5.

2.John M Senior, Optical Fiber Communications, Principles and Practice, 3rd Edition, Pearson Education, 2010, ISBN:978-81-317-3266-3

Reference Book:

Joseph C Palais, Fiber Optic Communication, Pearson Education, 2005, ISBN:0130085103.

BIOMEDICAL SIGNAL PROCESSING
VIII Semester EC

[As per Choice Based Credit System (CBCS)Scheme]

Course Code	18EC825	CIE Marks	40
Number of Lecture Hours/Week	3	SEE Marks	60
Total Number of Lecture Hours	40 (8 Hours/Module)	Exam Hours	03
CREDITS – 03			

Course Learning Objectives: This course will enable students to:

- Describe the origin, properties and suitable models of important biological signals such as ECG and EEG.
- Know the basic signal processing techniques in analysing biological signals.
- Acquire mathematical and computational skills relevant to the field of biomedical signal processing.
- Describe the basics of ECG signal compression algorithms.
- Know the complexity of various biological phenomena.
- Understand the promises, challenges of the biomedical engineering.

Module -1	RBT Level
Introduction to Biomedical Signals: The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis. **Electrocardiography:** Basic electrocardiography, ECG leads systems, ECG signal characteristics. **Signal Conversion** :Simple signal conversion systems, Conversion requirements for biomedical signals, Signal conversion circuits **(Text-1)**	**L1,L2**
Module -2	
Signal Averaging: Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. **Adaptive Noise Cancelling:** Principal noise canceller model, 60-Hz adaptive cancelling using a sine wave model, other applications of adaptive filtering **(Text-1)**	**L1,L2,L3**
Module -3	
Data Compression Techniques: Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding, data reduction algorithms The Fourier transform, Correlation, Convolution, Power spectrum estimation, Frequency domain analysis of the ECG **(Text-1)**	**L1,L2, L3**
Module -4	
Cardiological signal processing: Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Real-time ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor. **(Text -2)**	**L1,L2, L3**

Module -5	
Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. **Analysis of EEG channels:** Detection of EEG rhythms, Template matching for EEG, spike and wave detection **(Text-2)**	**L1,L2, L3**

Course outcomes: At the end of the course, students will be able to:

- Possess the basic mathematical, scientific and computational skills necessary to analyse ECG and EEG signals.
- Apply classical and modern filtering and compression techniques for ECG and EEG signals
- Develop a thorough understanding on basics of ECG and EEG feature extraction.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There willbe 2 full questions from each modulecovering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks willbe proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. **Biomedical Digital Signal Processing-** Willis J. Tompkins, PHI 2001.
2. **Biomedical Signal Processing Principles and Techniques-** D C Reddy, McGraw- Hill publications 2005.

Reference Book:

Biomedical Signal Analysis-Rangaraj M. Rangayyan, John Wiley & Sons 2002.